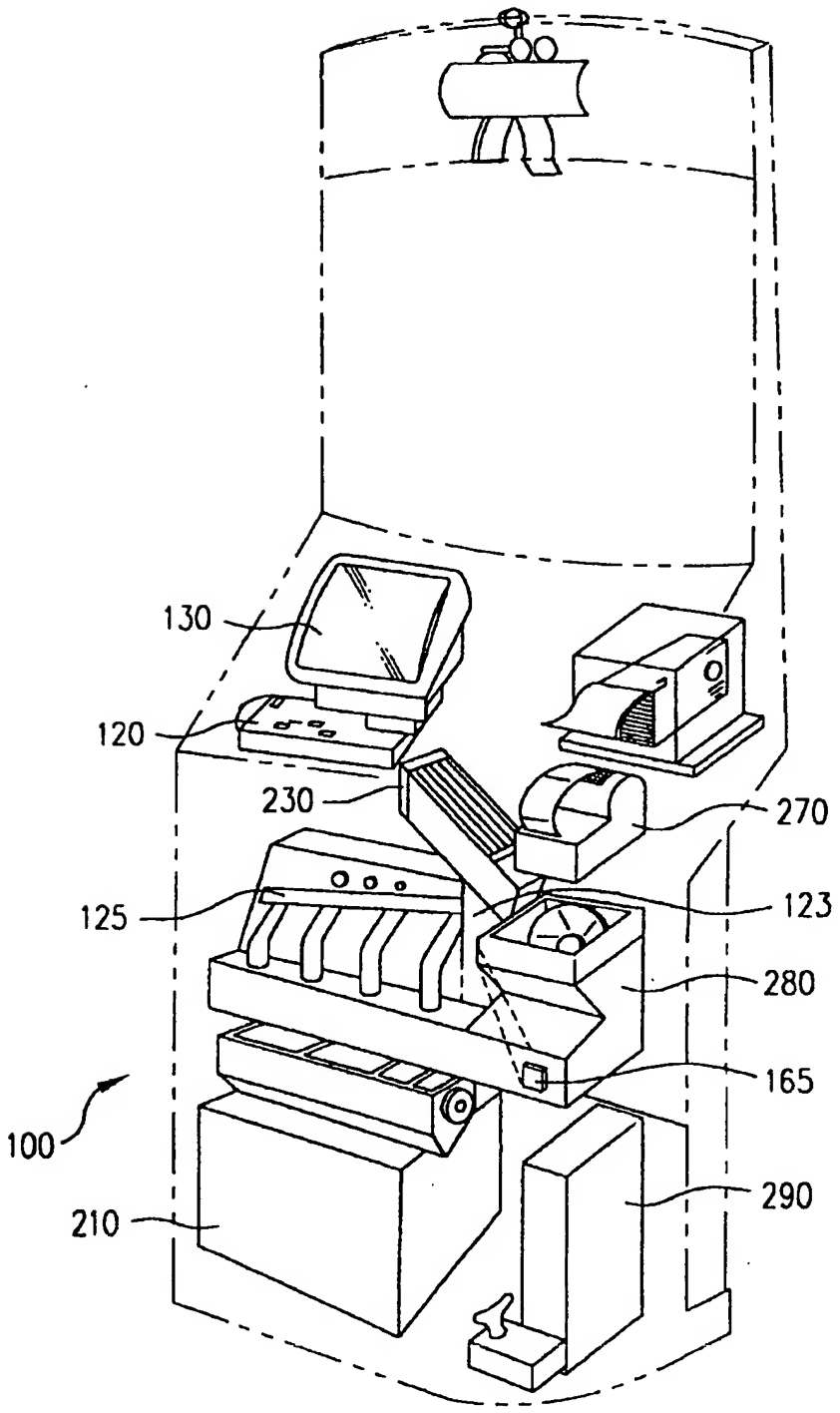


Fig. 1A

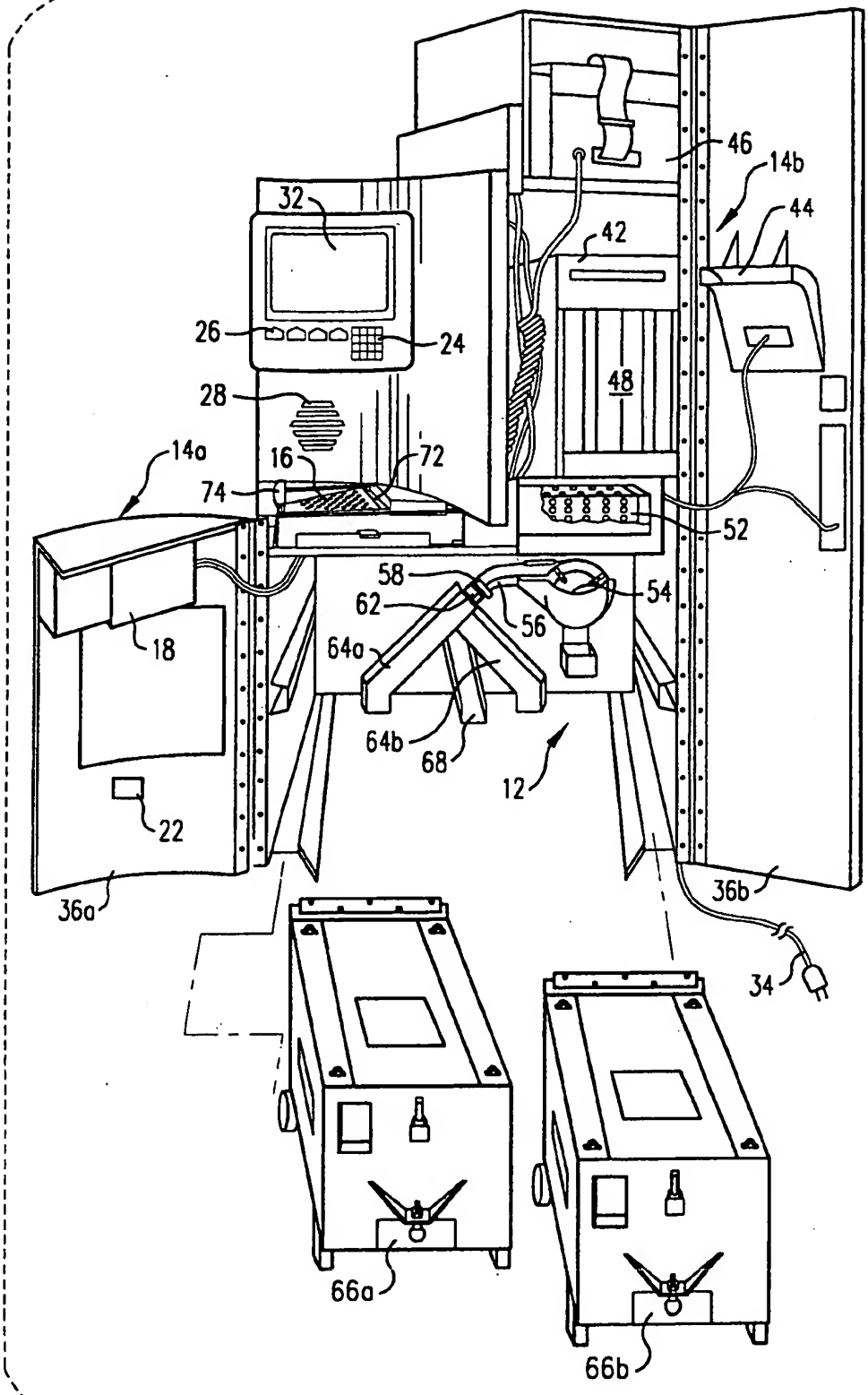

46
14b
44
32
42
26
24
48
28
14a
16
72
74
52
58
54
62
56
64a
18
64b
68
12
22
36a
36b
34
66a
66b

Fig. 1B

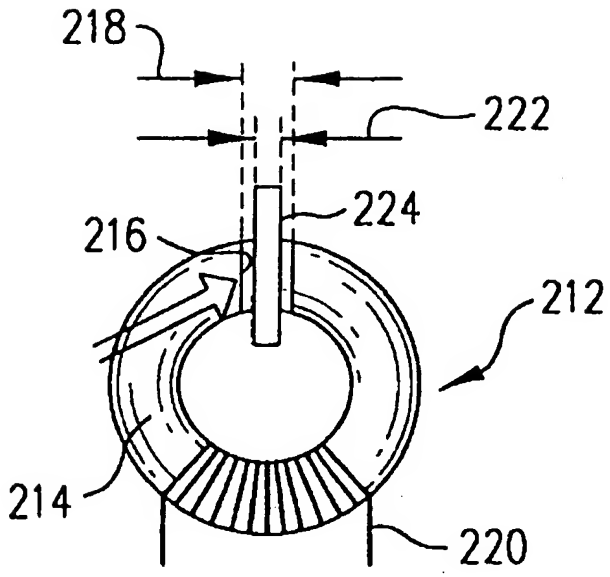

218
222
224
216
212
214
220

Fig. 2A

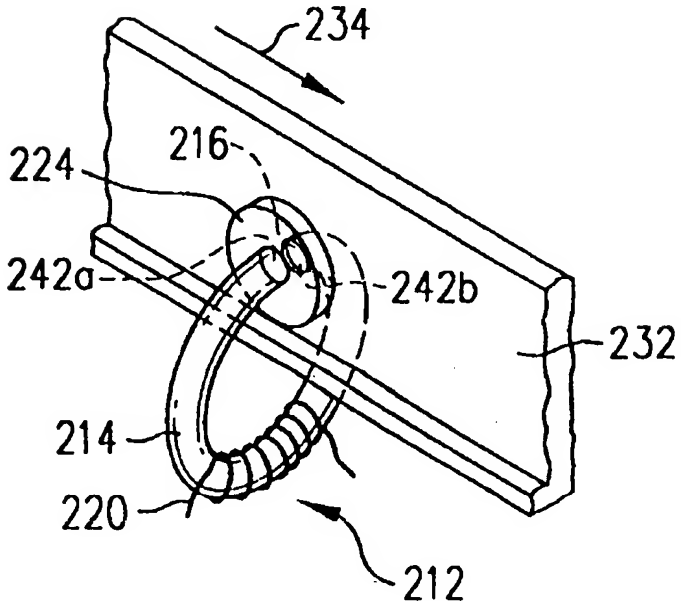

234
216
224
242a
242b
232
214
220
212

Fig. 2B

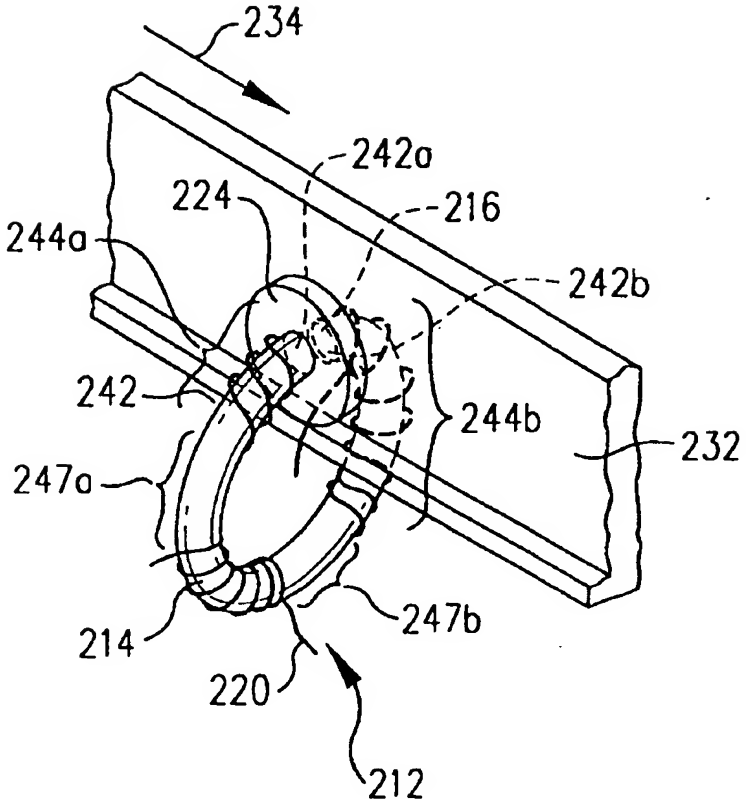

234
242a
224
216
244a
242b
242
244b
232
247a
247b
214
220
212

Fig. 2C

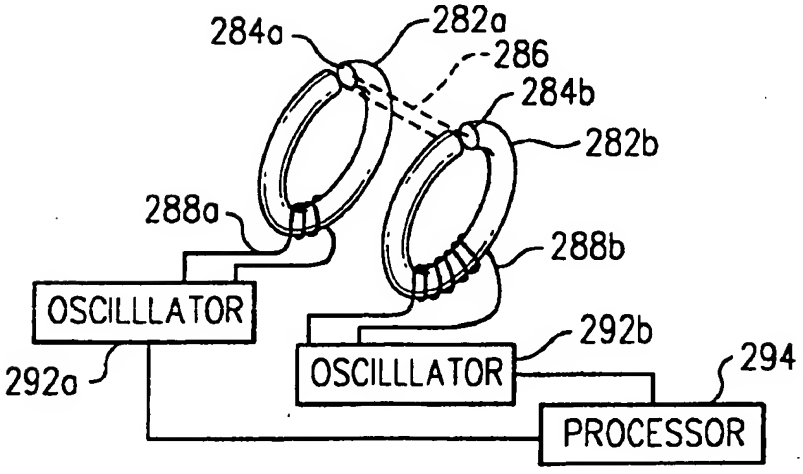

284a
282a
286
284b
282b
288a
288b
OSCILLLATOR
292a
OSCILLLATOR
292b
294
PROCESSOR

Fig. 2D

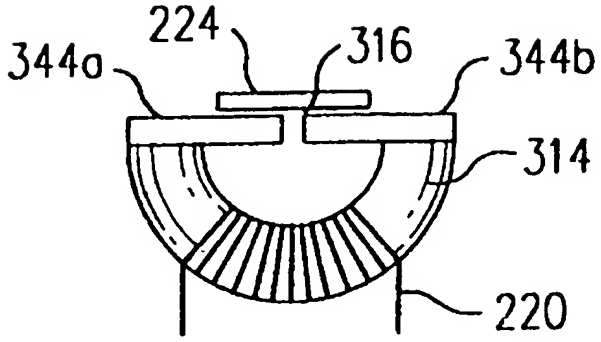


Fig. 3

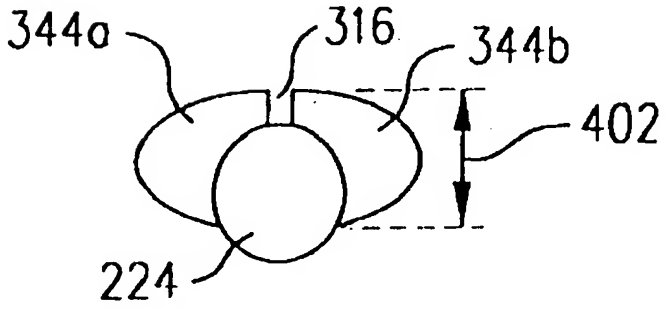


Fig. 4

FIG. 31A	FIG. 31B	FIG. 31C	FIG. 31D	FIG. 31E
	FIG. 31F	FIG. 31G	FIG. 31H	FIG. 31 I

Fig. 31

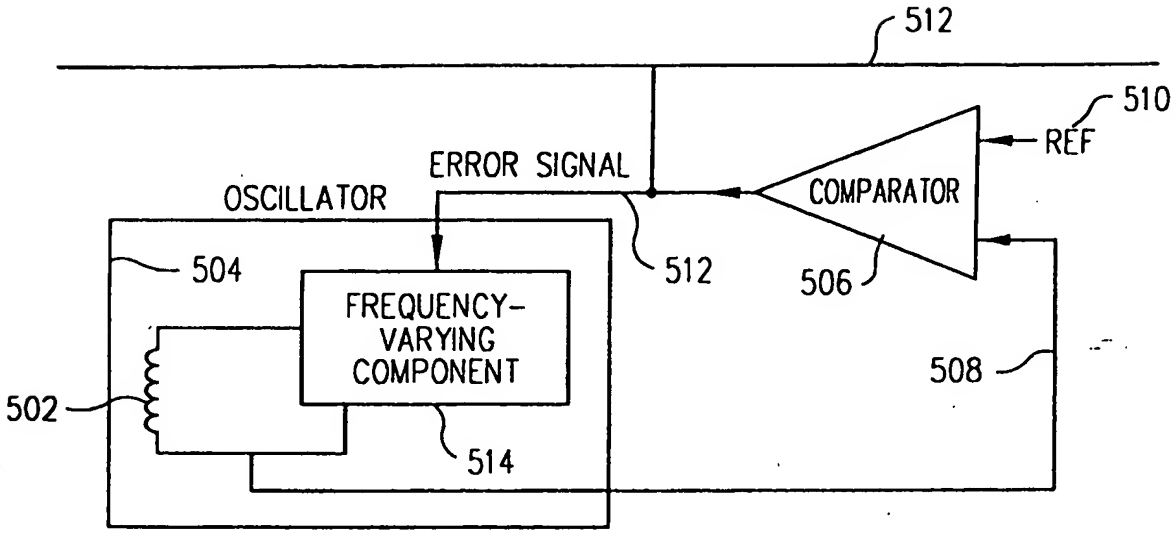

512
510
REF
ERROR SIGNAL
OSCILLATOR
COMPARATOR
504
512
506
FREQUENCY-
VARYING
COMPONENT
508
502
514

Fig. 5

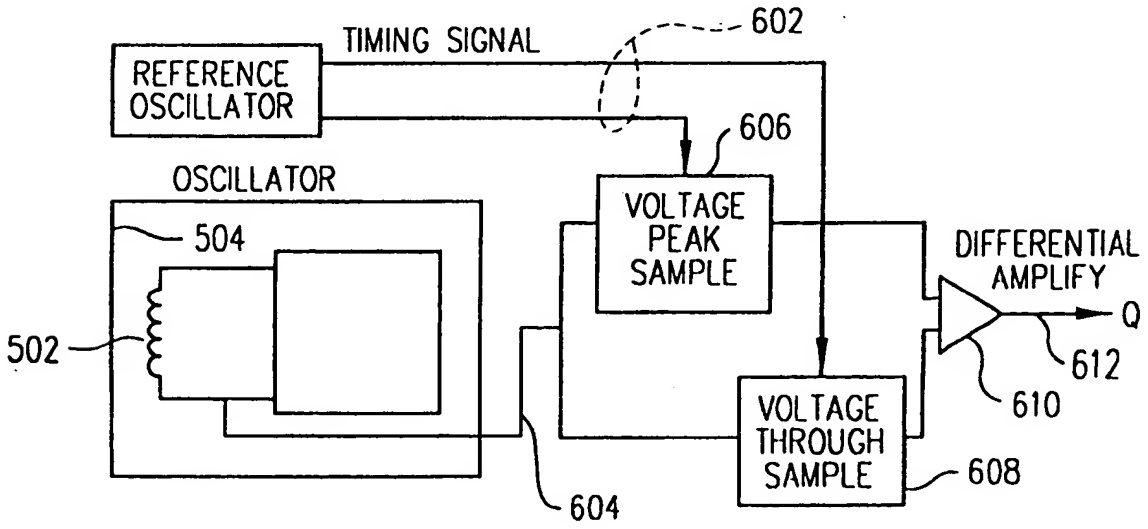

602
TIMING SIGNAL
REFERENCE
OSCILLATOR
606
OSCILLATOR
VOLTAGE
PEAK
SAMPLE
504
DIFFERENTIAL
AMPLIFY
Q
502
612
610
VOLTAGE
THROUGH
SAMPLE
608
604

Fig. 6

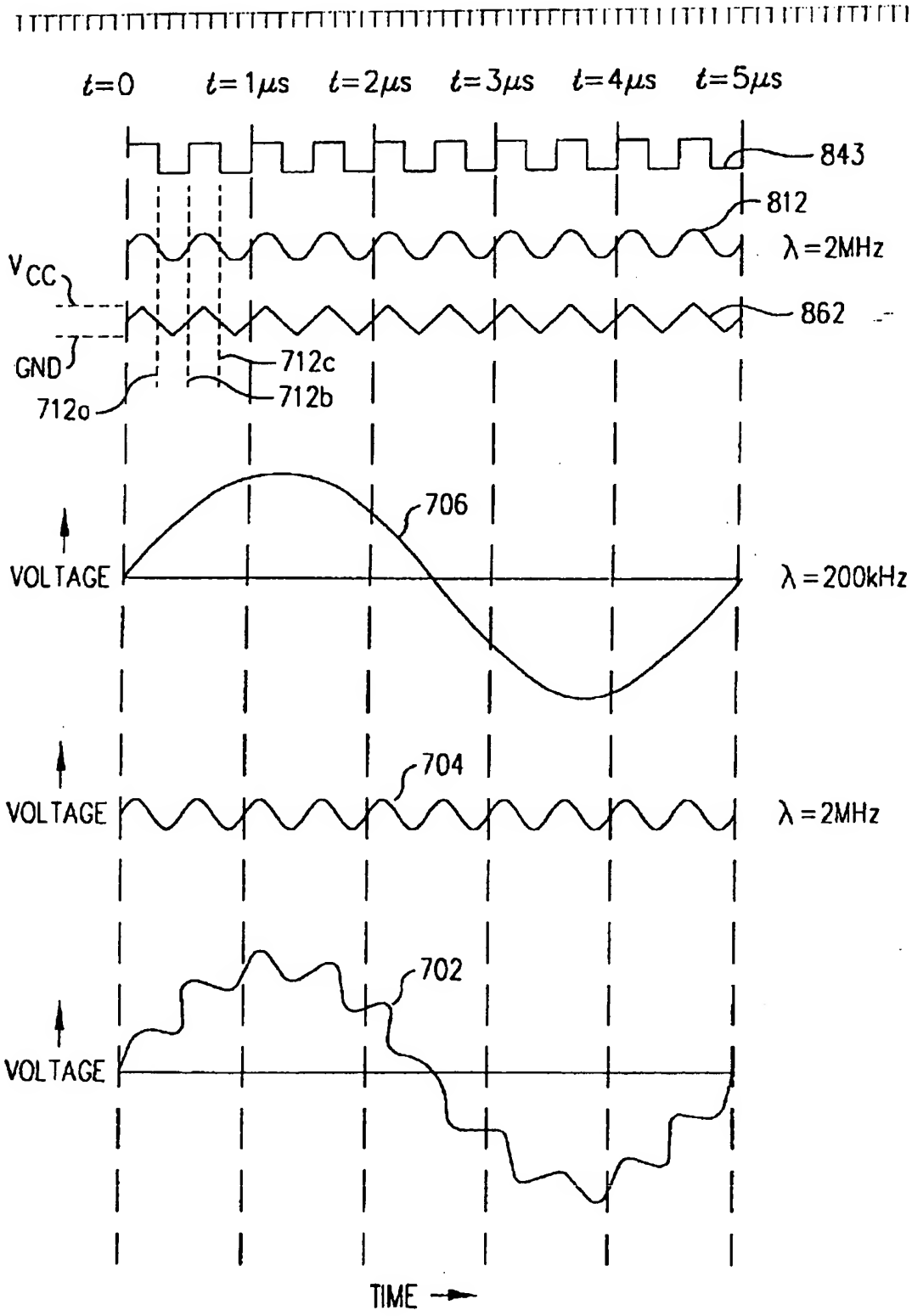

t=0
t=1μs
t=2μs
t=3μs
t=4μs
t=5μs
843
812
λ=2MHz
VCC
862
GND
712c
712b
712o
706
VOLTAGE
λ=200kHz
704
VOLTAGE
λ=2MHz
702
VOLTAGE
TIME

Fig. 7

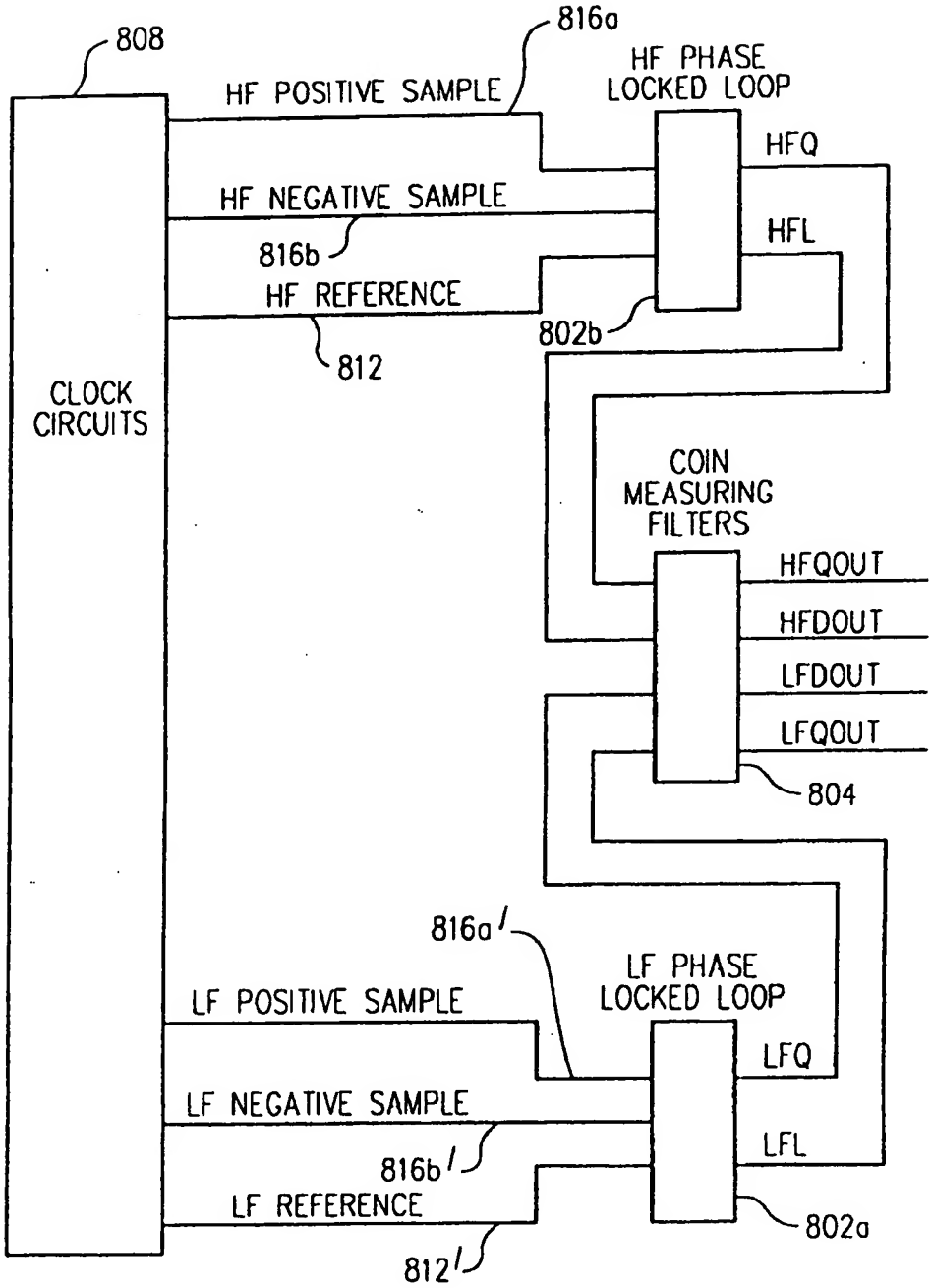

808
816a
HF POSITIVE SAMPLE
HF PHASE LOCKED LOOP
HFQ
HF NEGATIVE SAMPLE
HFL
816b
HF REFERENCE
802b
812
CLOCK CIRCUITS
COIN MEASURING FILTERS
HFQOUT
HFDOUT
LFDOUT
LFQOUT
804
816a'
LF PHASE LOCKED LOOP
LF POSITIVE SAMPLE
LFQ
LF NEGATIVE SAMPLE
LFL
816b'
LF REFERENCE
802a
812'

Fig. 8A

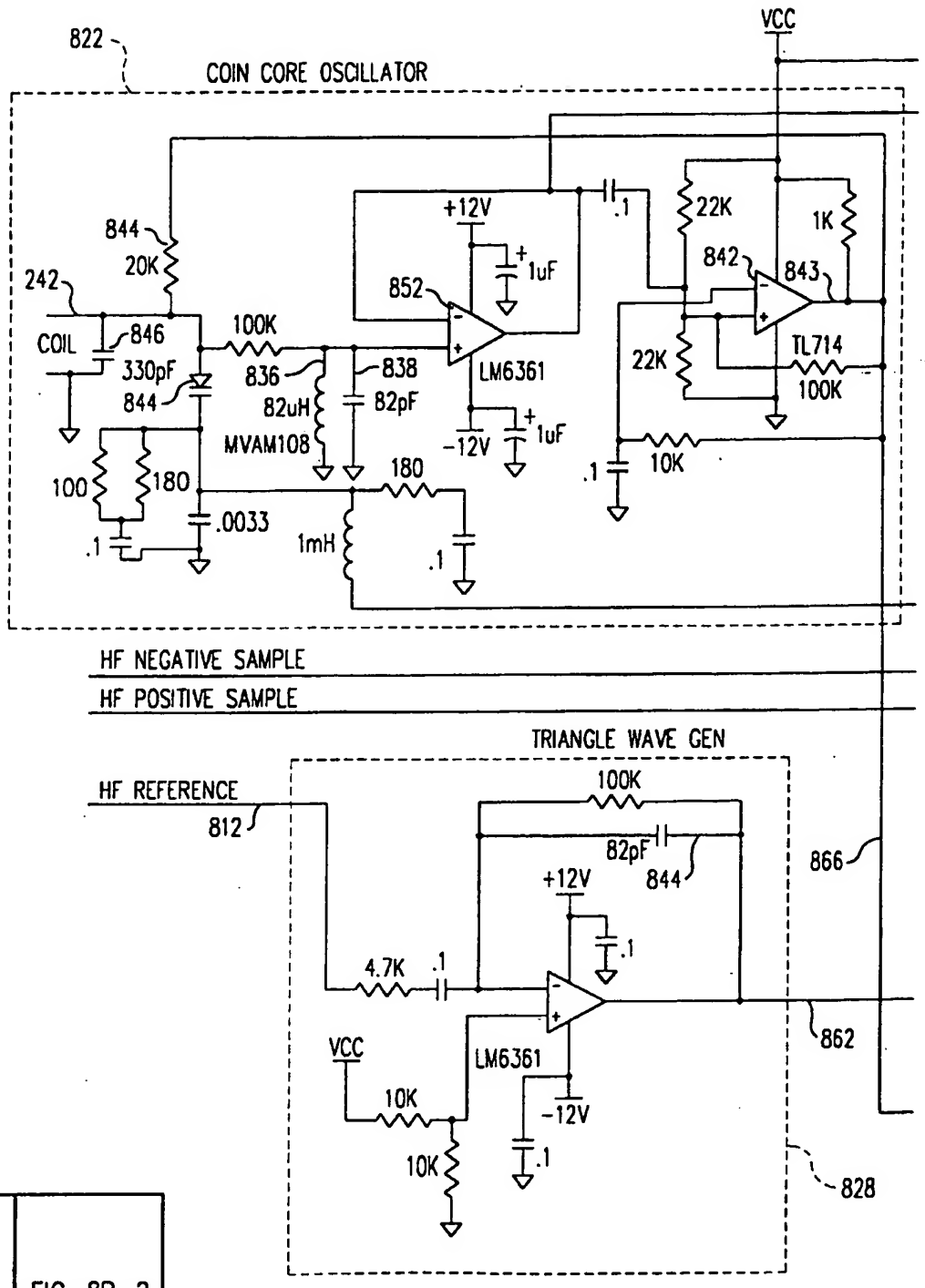


Fig. 8B-1

FIG. 8B-1	FIG. 8B-2

Fig. 8B

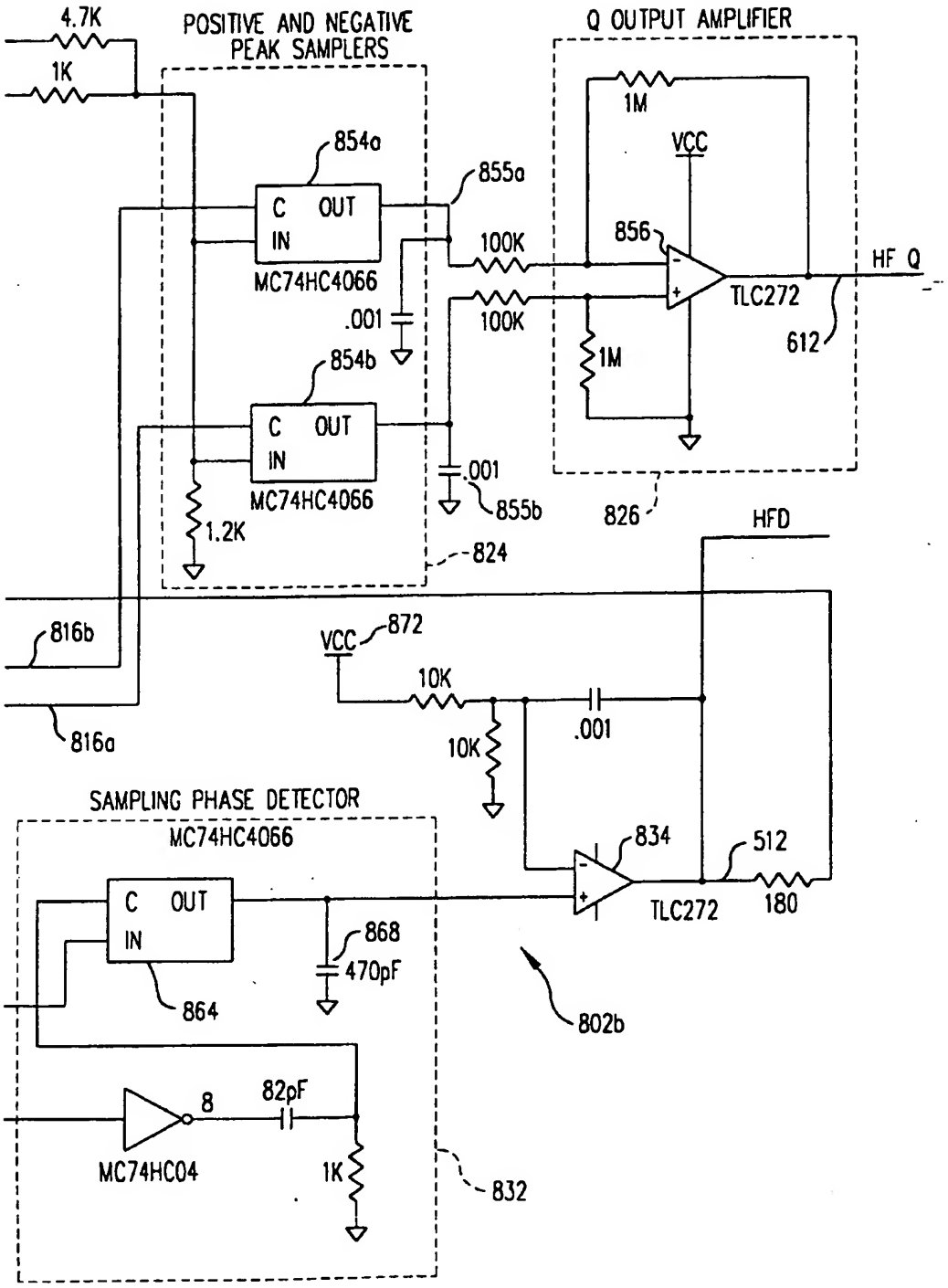

4.7K
1K
POSITIVE AND NEGATIVE
PEAK SAMPLERS
Q OUTPUT AMPLIFIER
1M
VCC
854a
855a
C OUT
IN
MC74HC4066
100K
856
HF Q
TLC272
.001
100K
612
1M
854b
C OUT
IN
MC74HC4066
.001
855b
826
1.2K
824
HFD
816b
VCC
872
10K
.001
816a
10K
SAMPLING PHASE DETECTOR
MC74HC4066
834
512
C OUT
IN
TLC272
180
868
470pF
802b
864
8
82pF
MC74HC04
1K
832

Fig. 8B-2

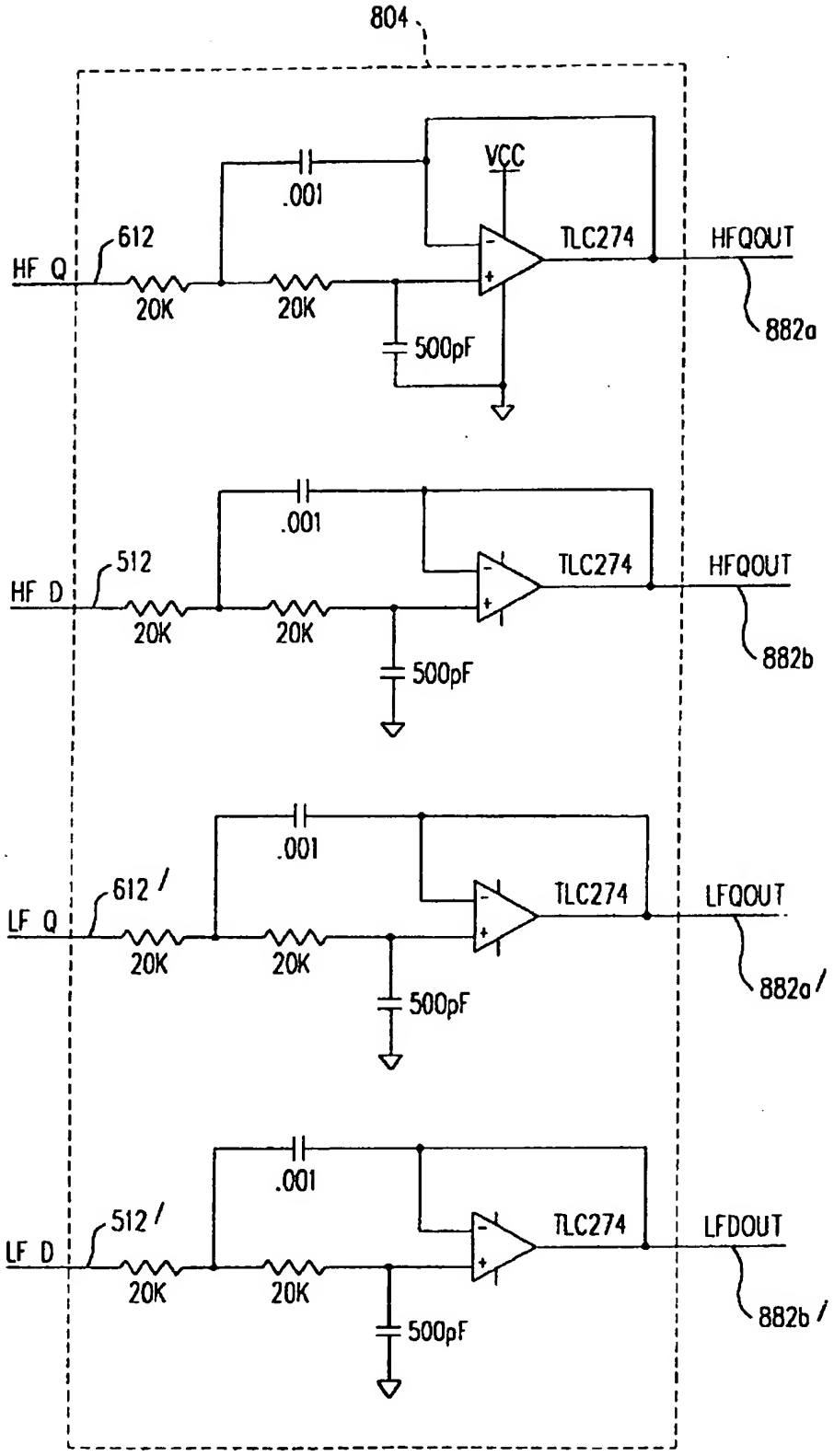

804
VCC
.001
612
HF Q
20K
20K
TLC274
HFQOUT
882a
500pF
.001
512
HF D
20K
20K
TLC274
HFQOUT
882b
500pF
.001
612 /
LF Q
20K
20K
TLC274
LFQOUT
882a /
500pF
.001
512 /
LF D
20K
20K
TLC274
LFDOUT
882b /
500pF

Fig. 8C

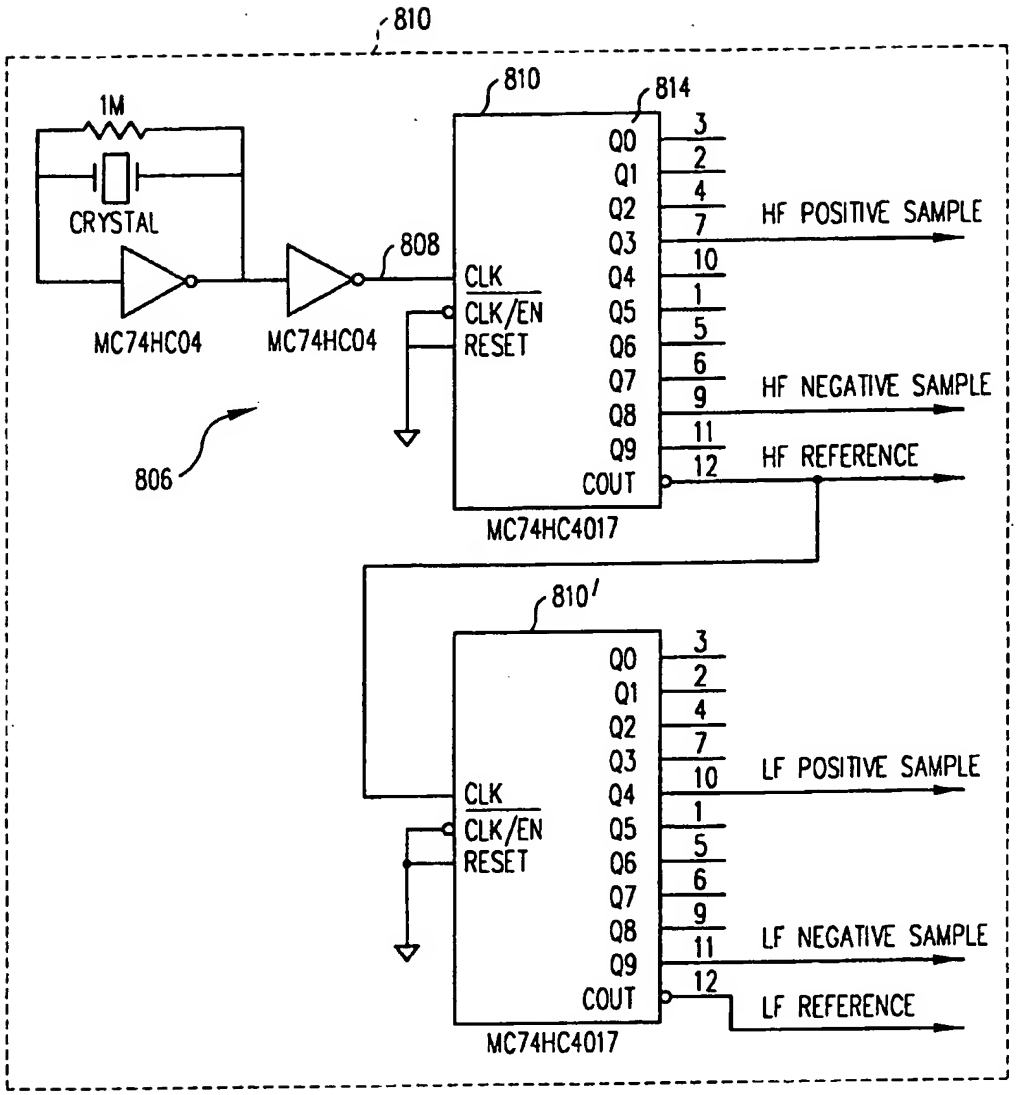

810
1M
CRYSTAL
MC74HC04
MC74HC04
808
806
810
814
CLK
CLK/EN
RESET
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
COUT
3
2
4
7
10
1
5
6
9
11
12
HF POSITIVE SAMPLE
HF NEGATIVE SAMPLE
HF REFERENCE
MC74HC4017
810'
CLK
CLK/EN
RESET
LF POSITIVE SAMPLE
LF NEGATIVE SAMPLE
LF REFERENCE
MC74HC4017

Fig. 8D

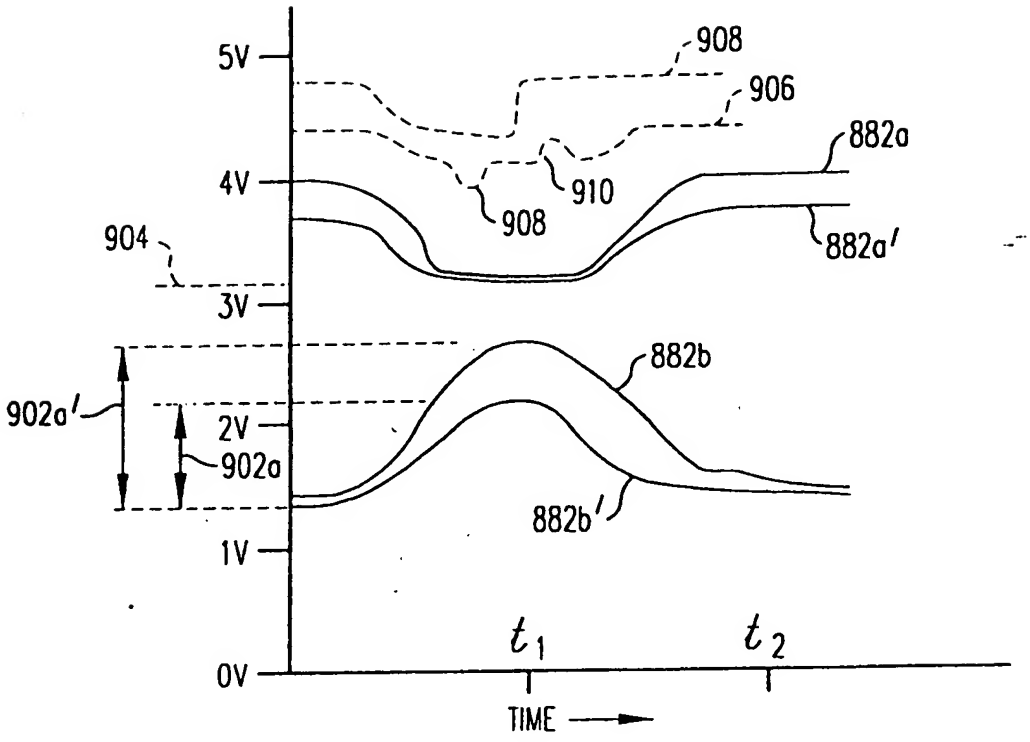

5V
4V
3V
2V
1V
0V
908
906
882a
910
908
882a'
904
882b
902a'
902a
882b'
t_1
t_2
TIME

Fig. 9

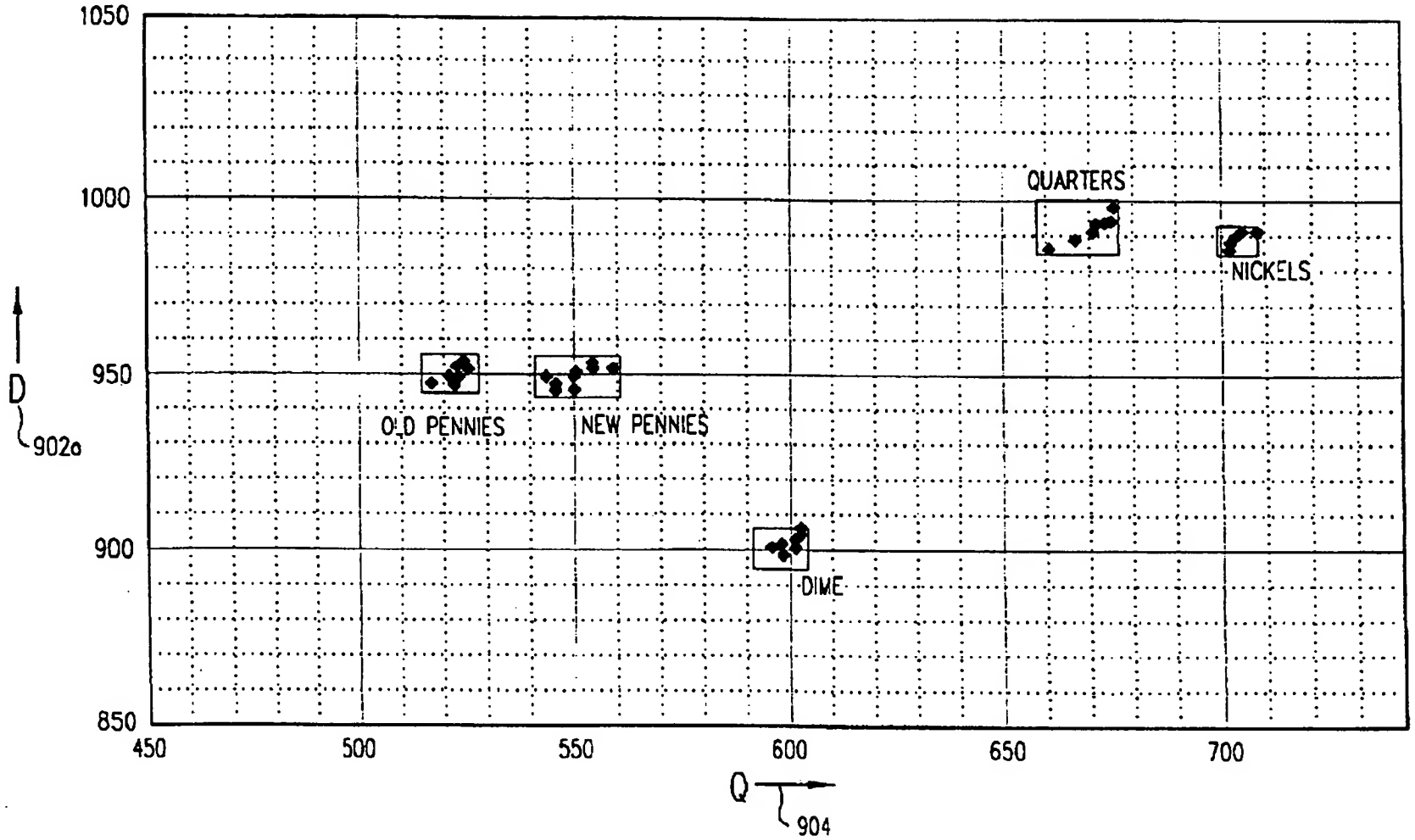

1050
1000
950
900
850
D
902a
450
500
550
600
650
700
Q
904
QUARTERS
NICKELS
OLD PENNIES
NEW PENNIES
DIME

Fig. 10A

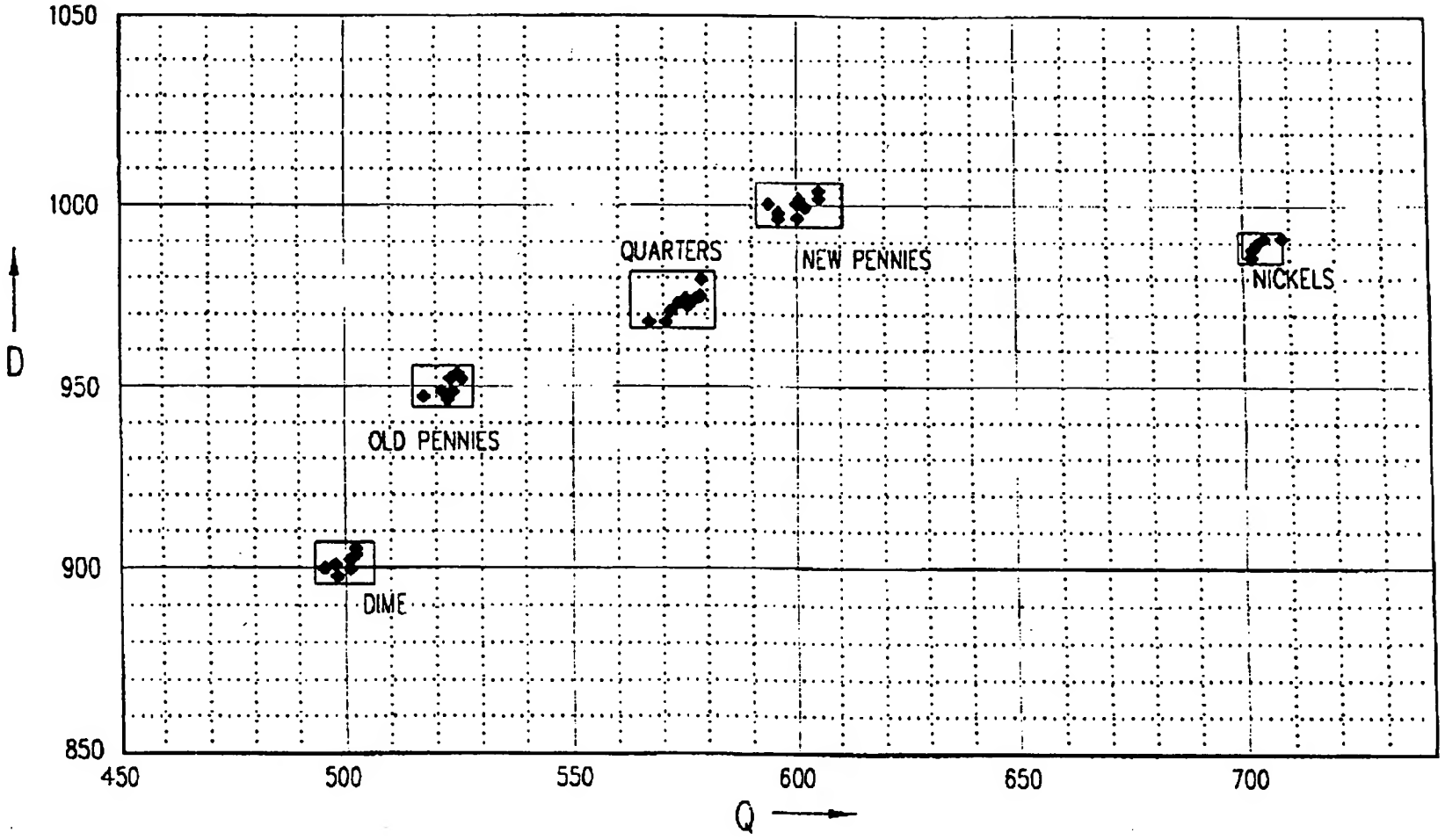

1050
1000
950
900
850
D
450
500
550
600
650
700
Q
QUARTERS
NEW PENNIES
NICKELS
OLD PENNIES
DIME

Fig. 10B

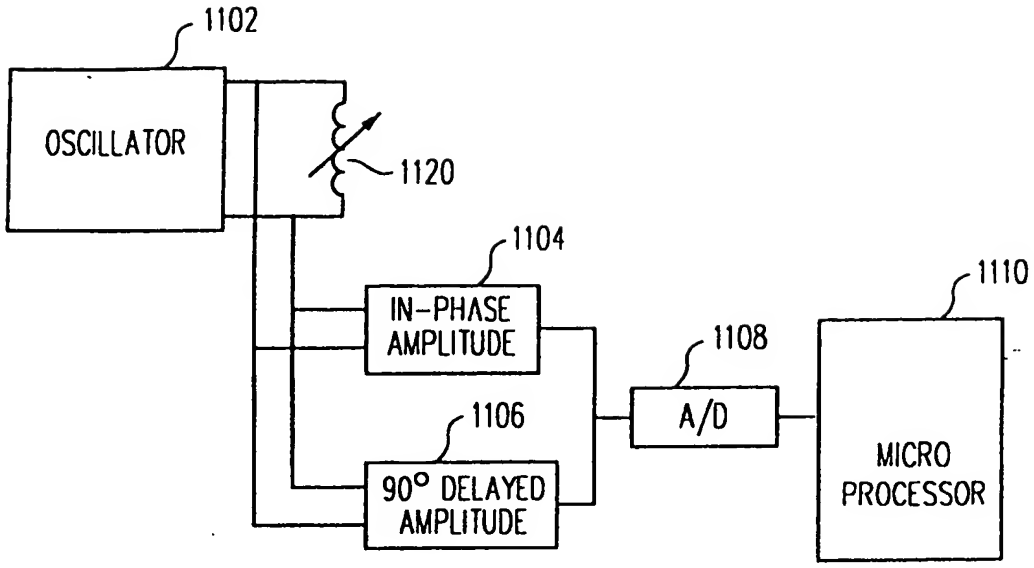

1102
OSCILLATOR
1120
1104
IN-PHASE AMPLITUDE
1110
1108
A/D
1106
90° DELAYED AMPLITUDE
MICRO PROCESSOR

Fig. 11

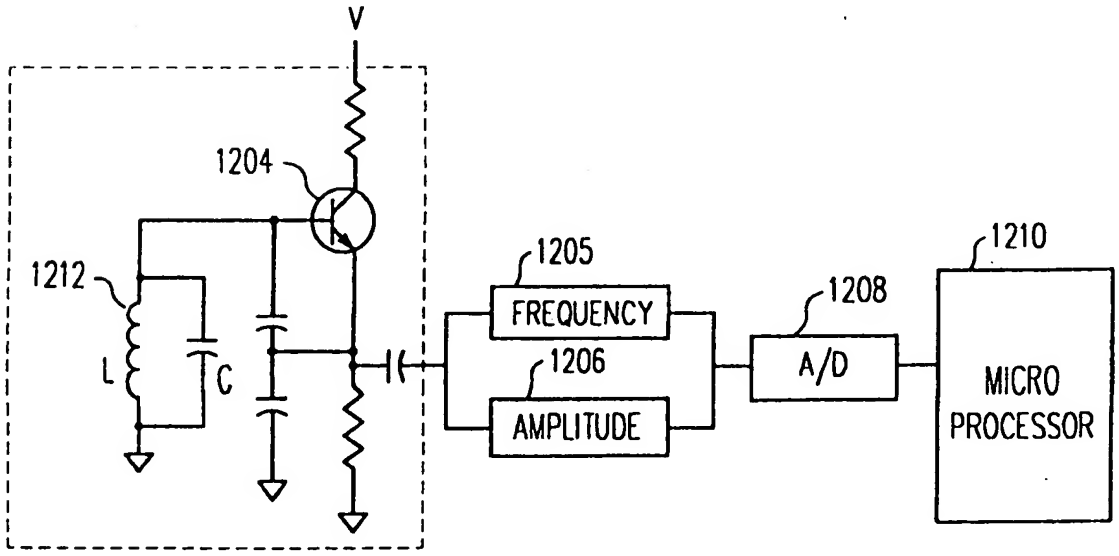

V
1204
1212
L
C
1205
FREQUENCY
1206
AMPLITUDE
1208
A/D
1210
MICRO PROCESSOR

Fig. 12

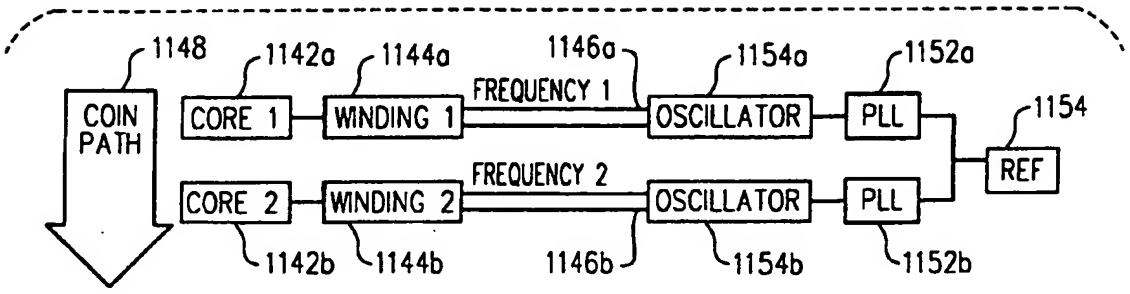

1148
COIN PATH
1142a
CORE 1
1144a
WINDING 1
1146a
FREQUENCY 1
1154a
OSCILLATOR
1152a
PLL
1154
REF
CORE 2
1142b
WINDING 2
1144b
FREQUENCY 2
1146b
OSCILLATOR
1154b
PLL
1152b

Fig. 11A

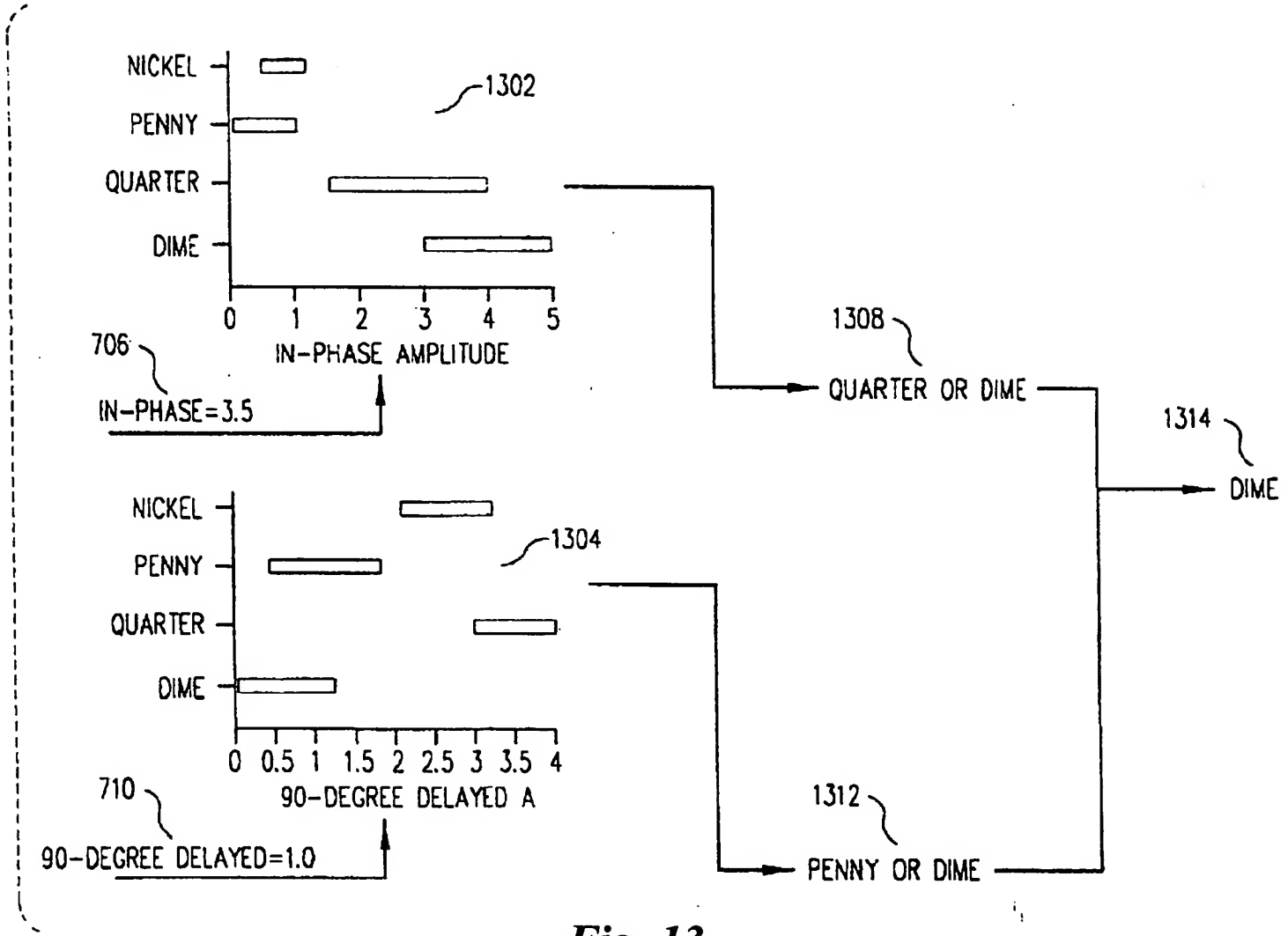

NICKEL
PENNY
QUARTER
DIME
1302
0 1 2 3 4 5
IN-PHASE AMPLITUDE
706
IN-PHASE=3.5
1308
QUARTER OR DIME
1314
DIME
NICKEL
PENNY
QUARTER
DIME
1304
0 0.5 1 1.5 2 2.5 3 3.5 4
90-DEGREE DELAYED A
710
90-DEGREE DELAYED=1.0
1312
PENNY OR DIME

Fig. 13

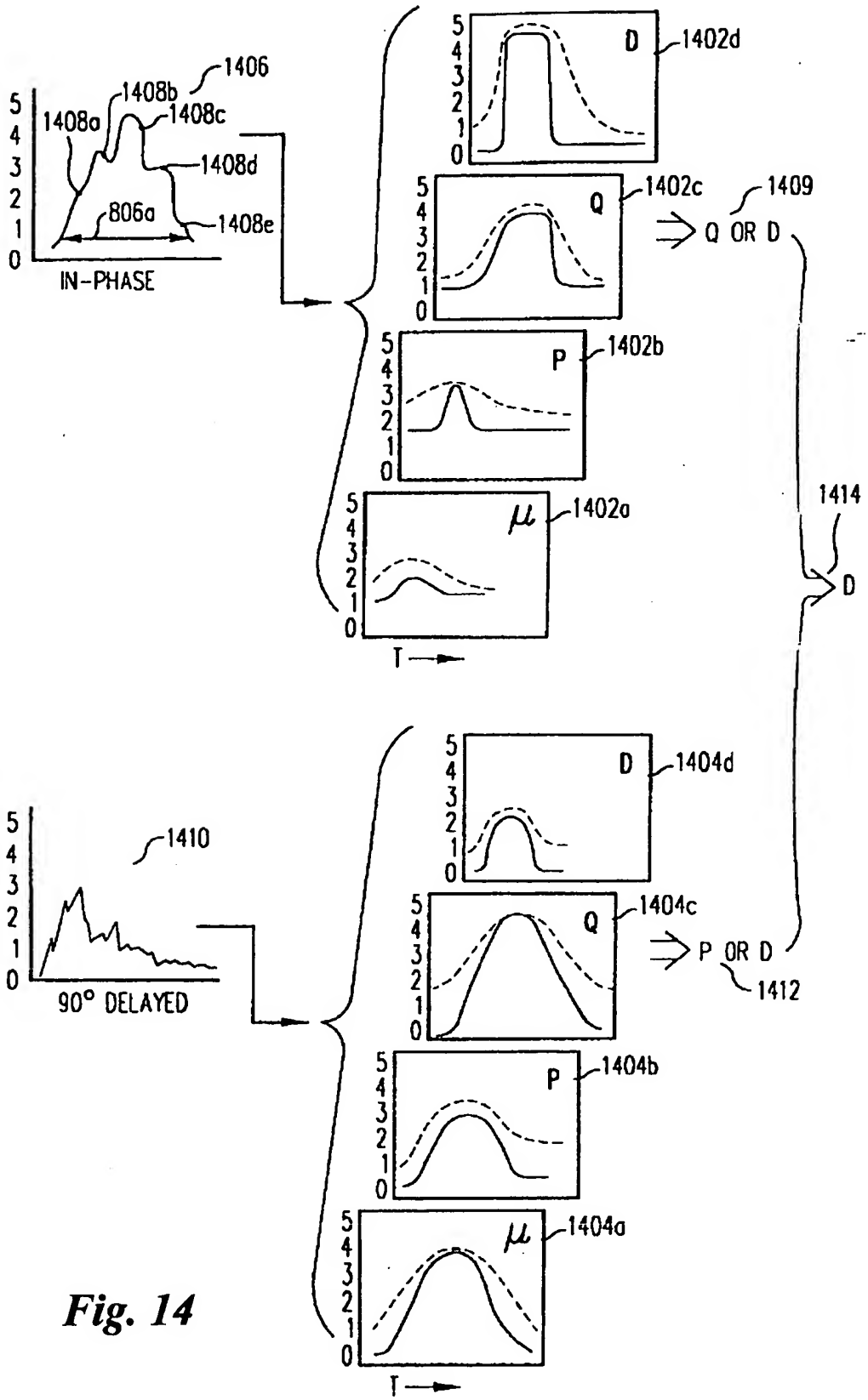

1406
1408a
1408b
1408c
1408d
1408e
806a
IN-PHASE
1402d
D
1402c
Q
1409
Q OR D
1402b
P
1402a
μ
1414
D
T
1410
90° DELAYED
1404d
D
1404c
Q
P OR D
1412
1404b
P
1404a
μ
T

Fig. 14

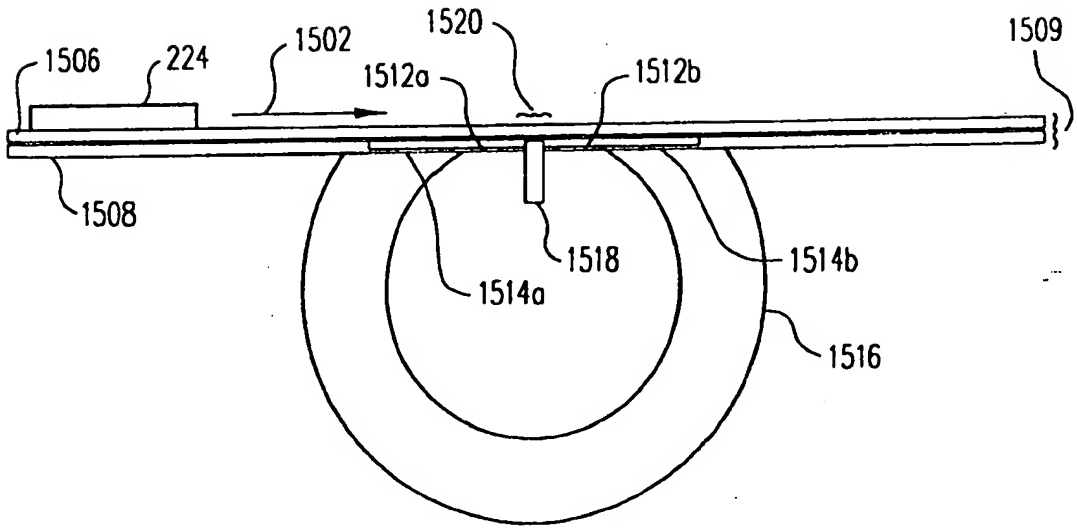


Fig. 15A

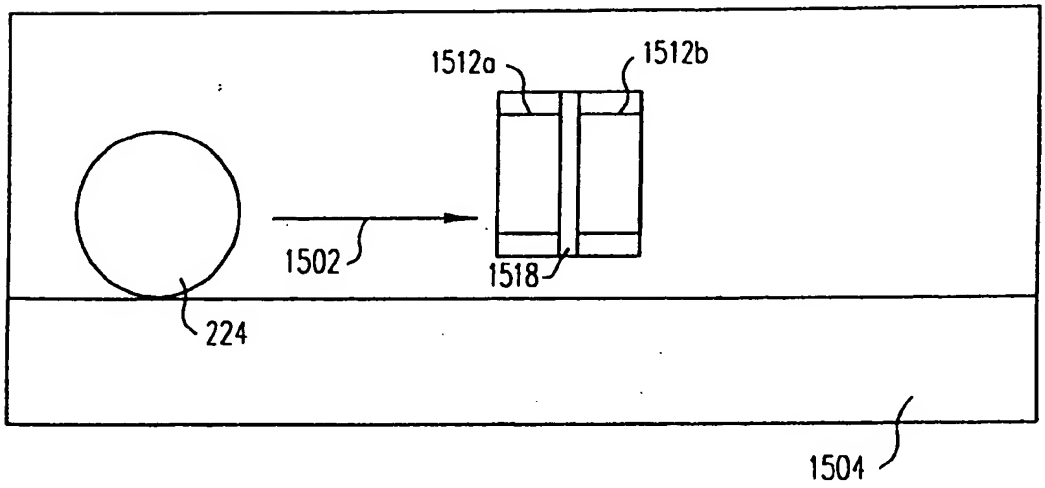


Fig. 15B

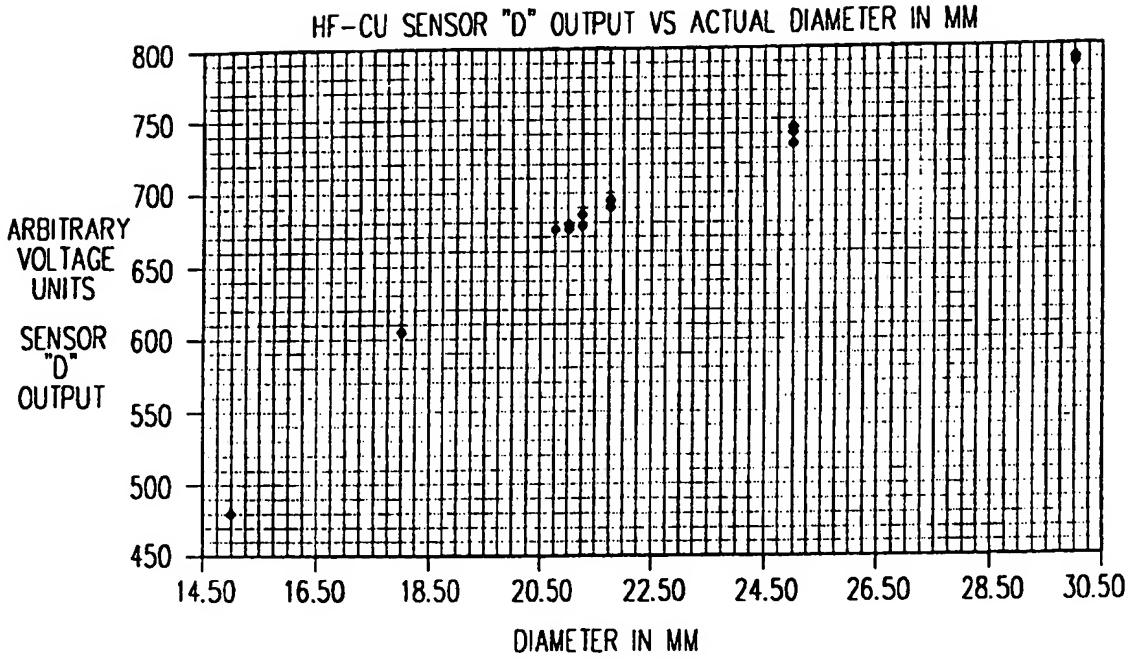


Fig. 16A

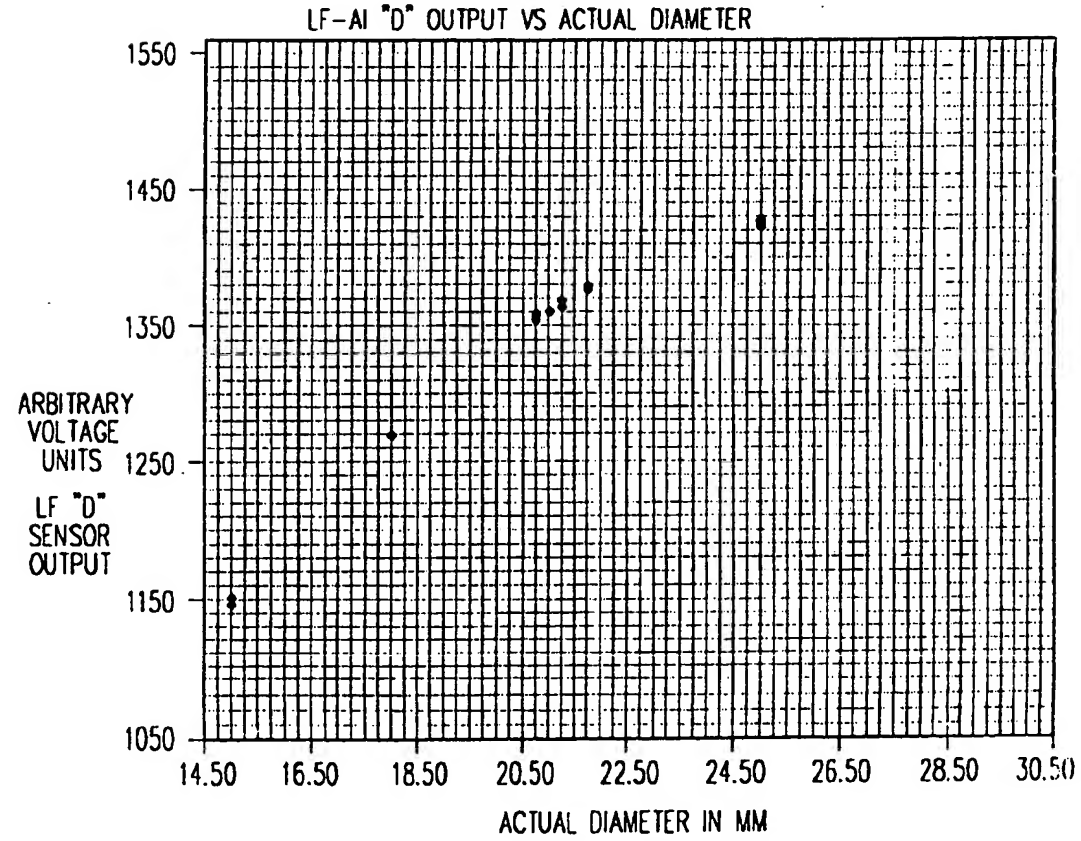


Fig. 16B

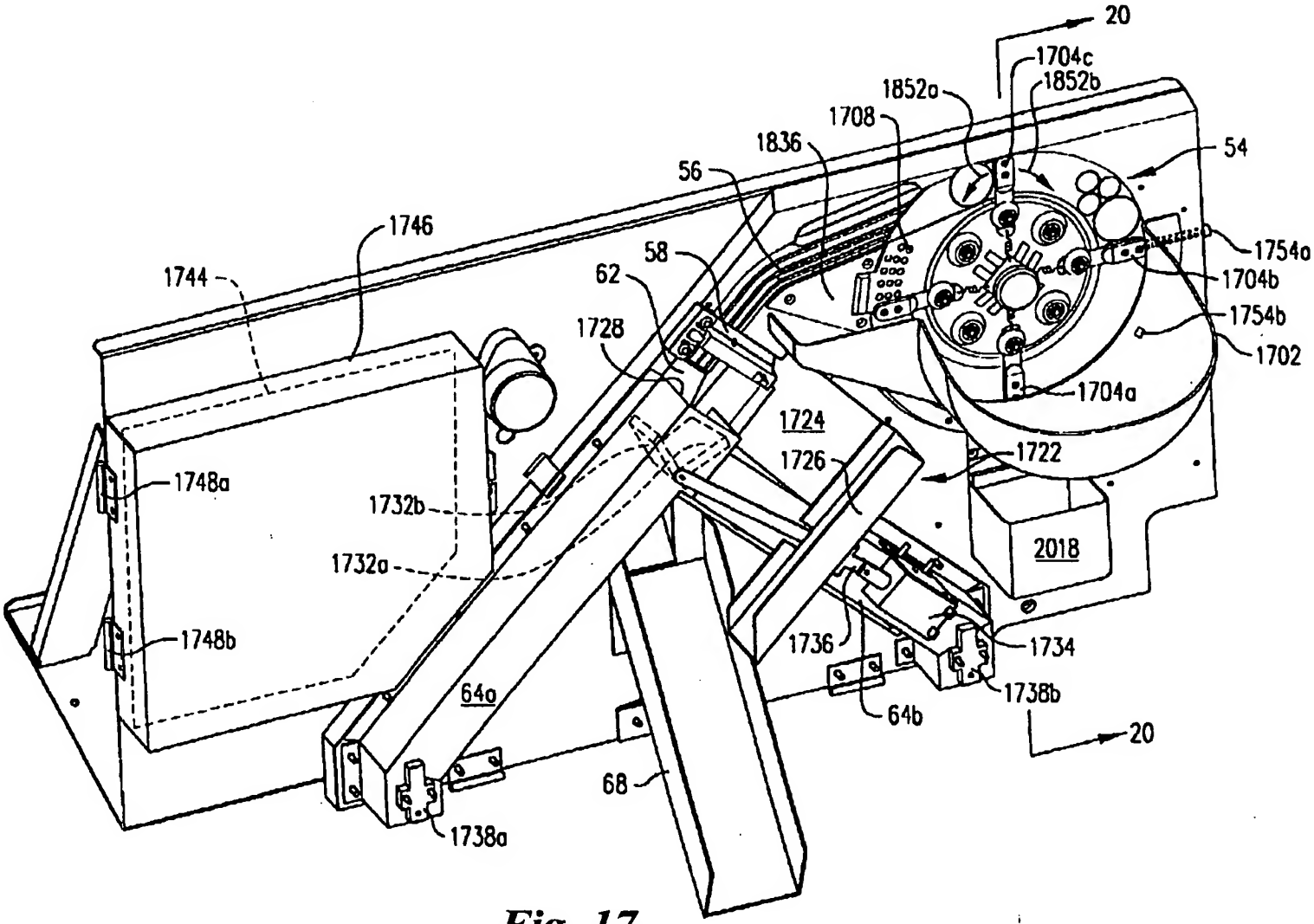

20
1704c
1852b
1852a
1708
1836
56
54
1746
1744
58
62
1754a
1704b
1754b
1728
1702
1704a
1724
1722
1726
1748a
1732b
1732a
2018
1748b
1736
1734
64a
1738b
64b
20
68
1738a

Fig. 17

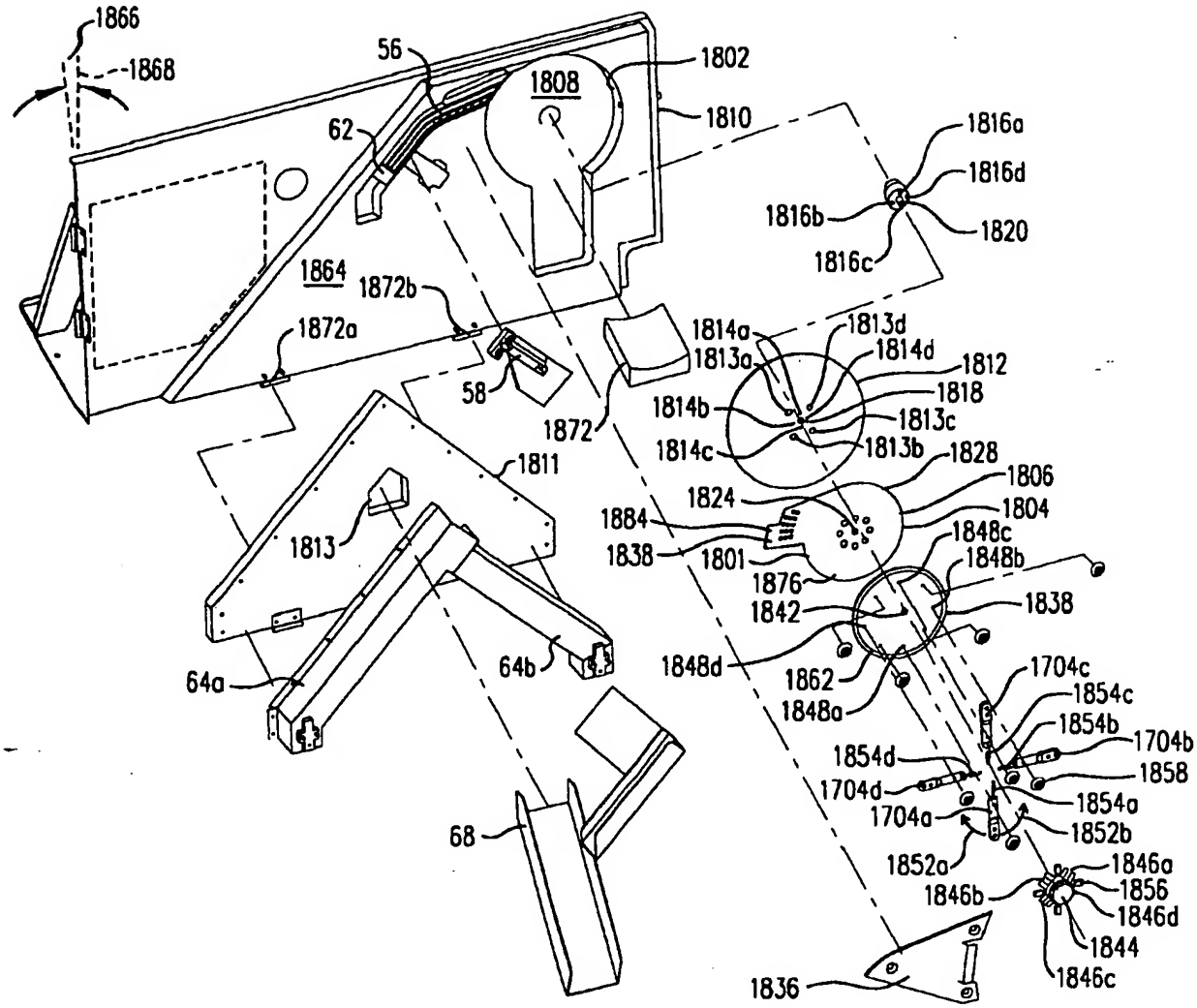


Fig. 18

FIG. 35A	FIG. 35B

Fig. 35

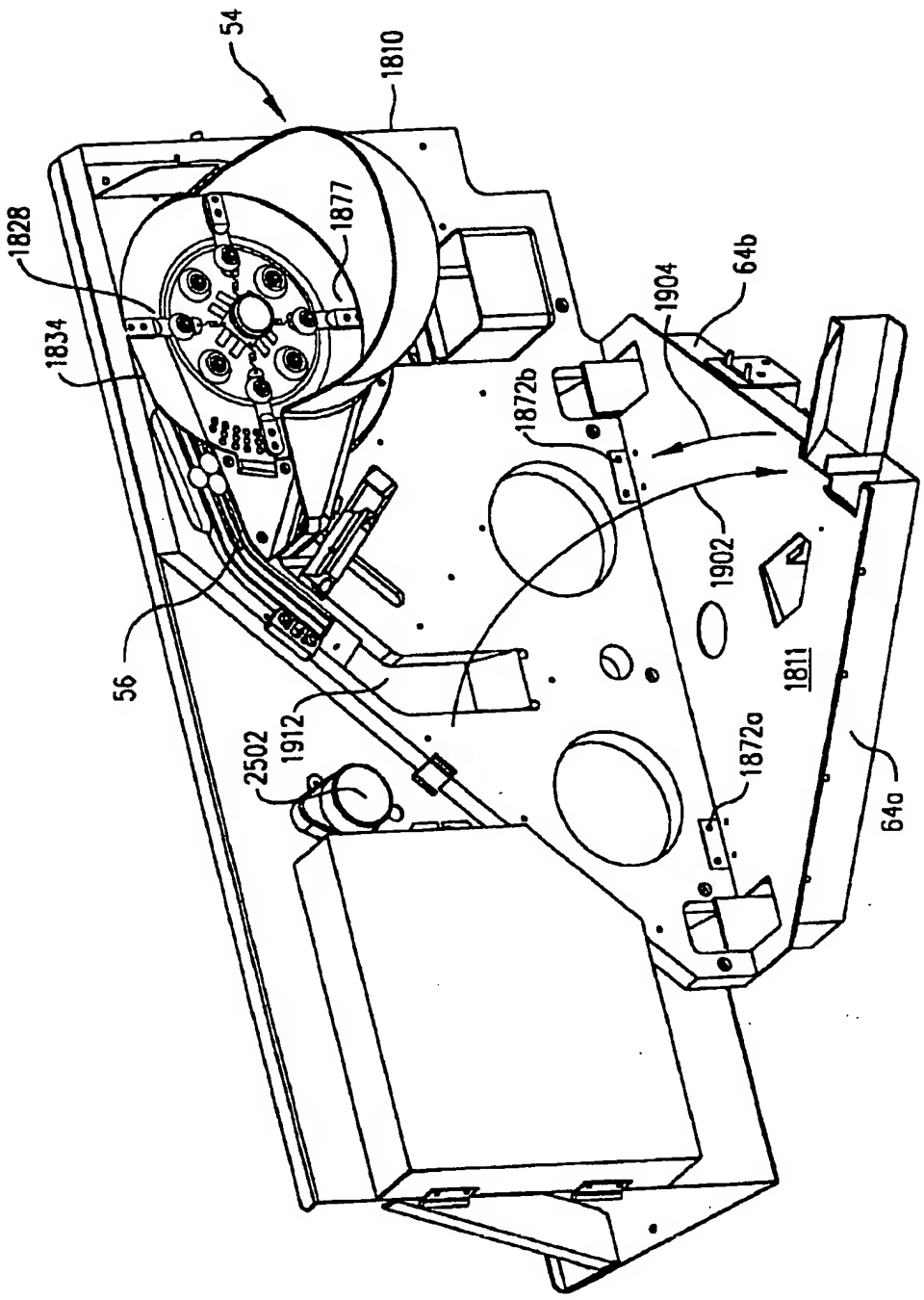

54
1810
1828
1877
1834
1904
64b
1872b
1902
56
1811
2502
1912
1872a
64a

Fig. 19

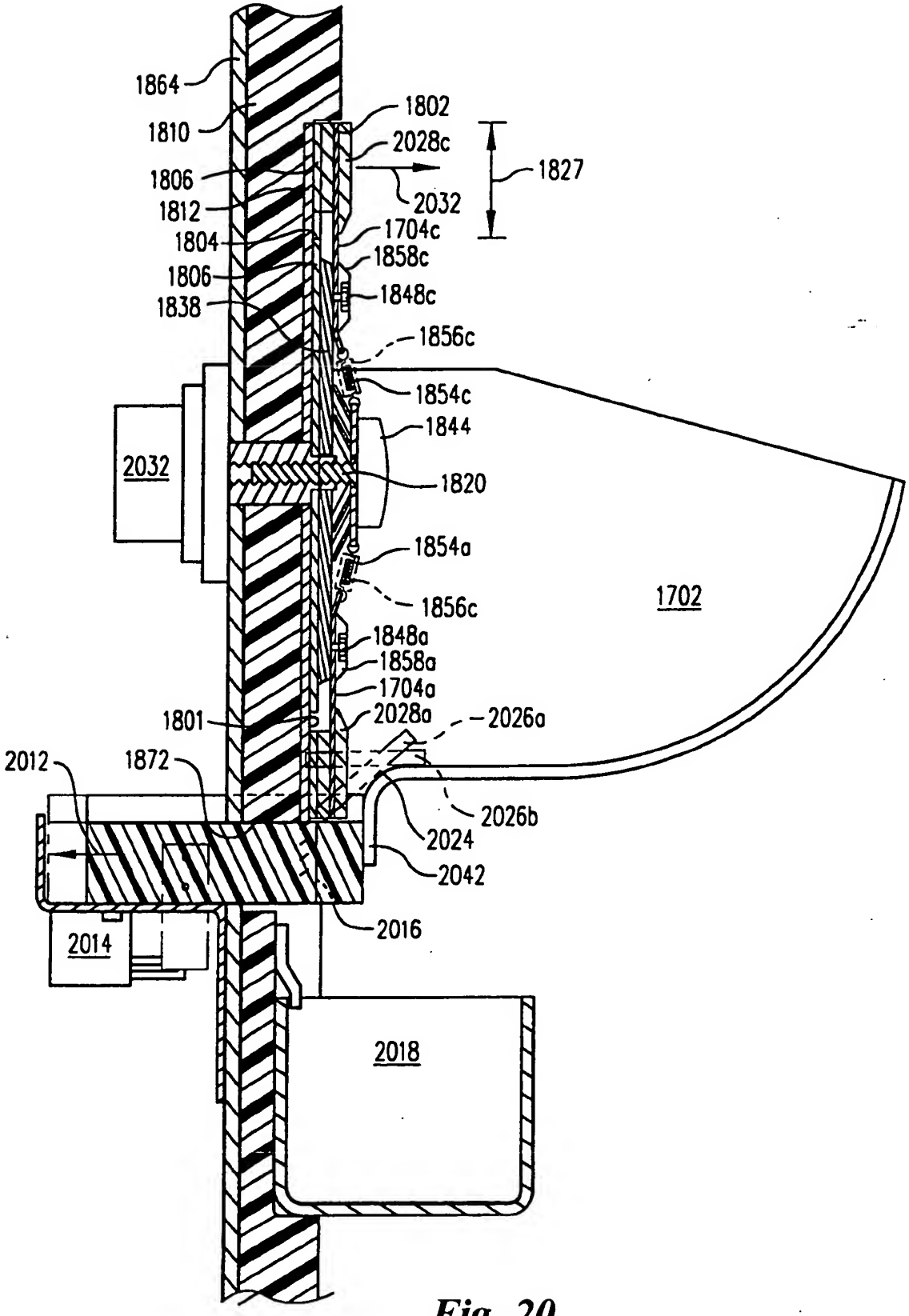

1864
1810
1806
1812
1804
1806
1838
1802
2028c
2032
1827
1704c
1858c
1848c
1856c
1854c
1844
1820
1854a
1856c
1848a
1858a
1704a
2028a
2026a
1801
2012
1872
2026b
2024
2042
2016
2014
2018
2032
1702

Fig. 20

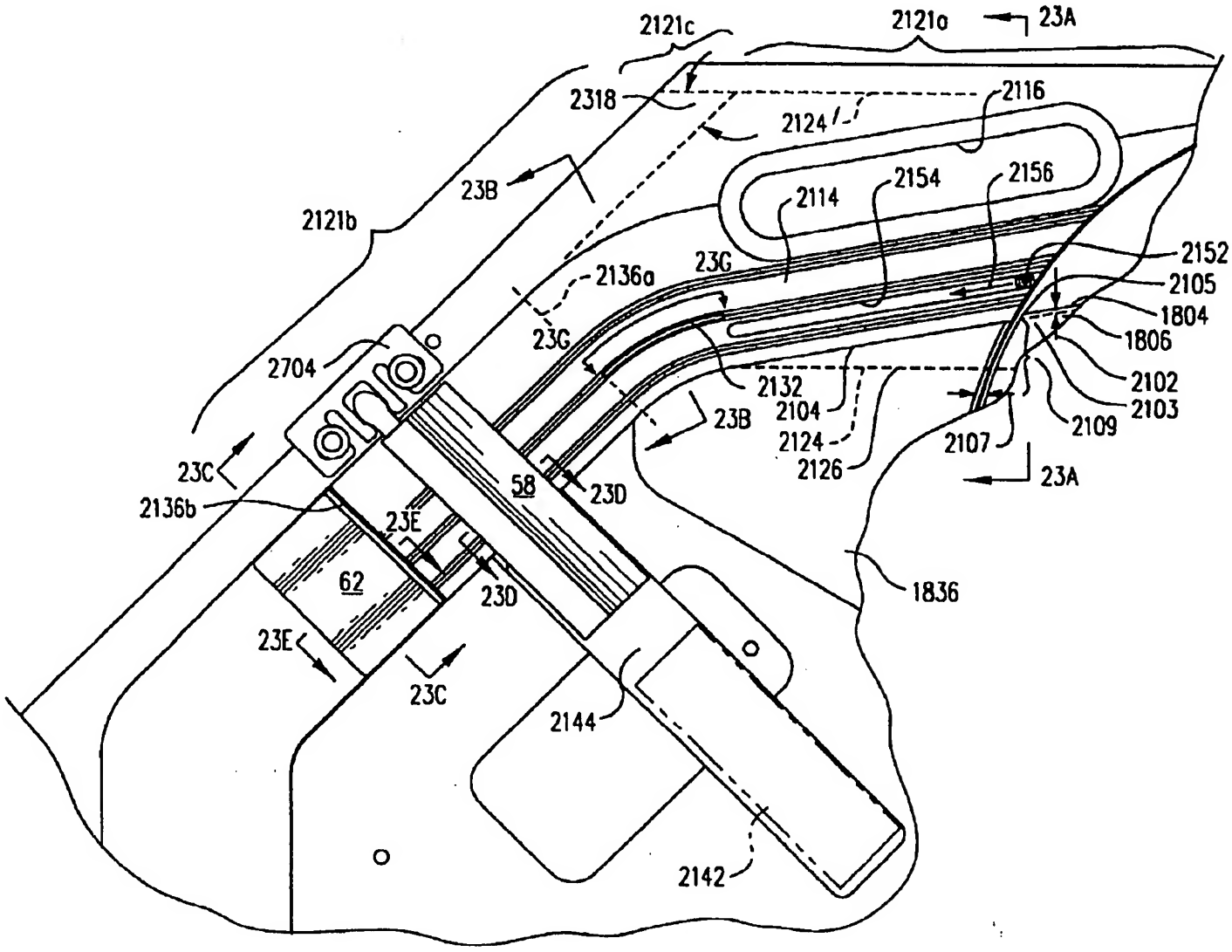

2121c
2121a
23A
2318
2116
2124
23B
2121b
2114
2154
2156
2152
2136a
23G
2105
1804
1806
2704
2102
2103
2132
2104
2124
2126
2109
2107
23C
58
23D
2136b
23E
62
1836
23E
23C
2144
2142

Fig. 21

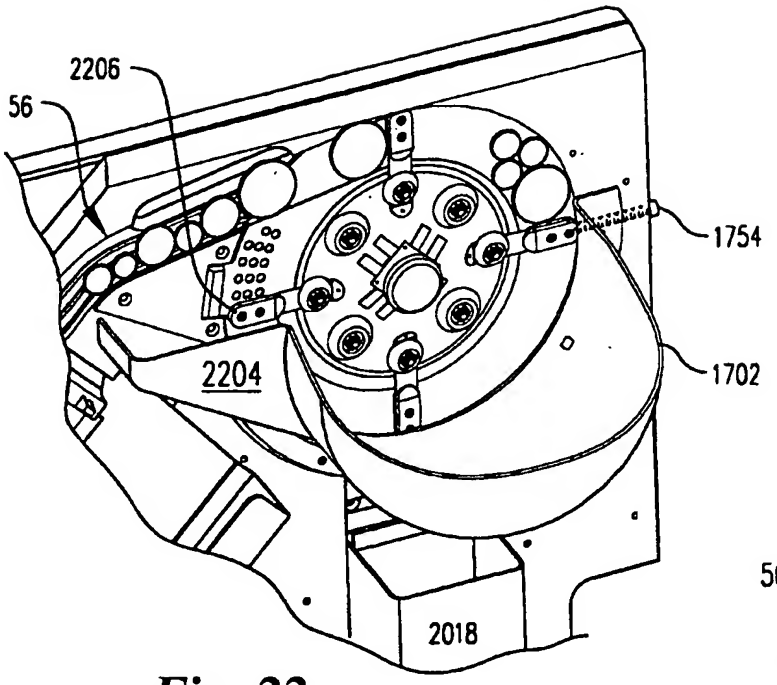
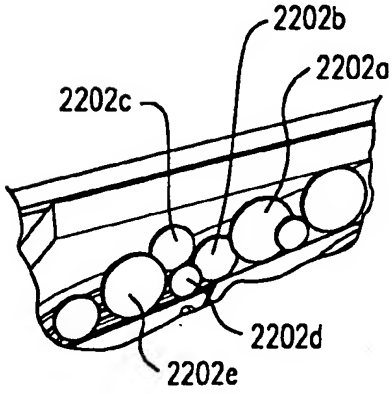


Fig. 22



22A

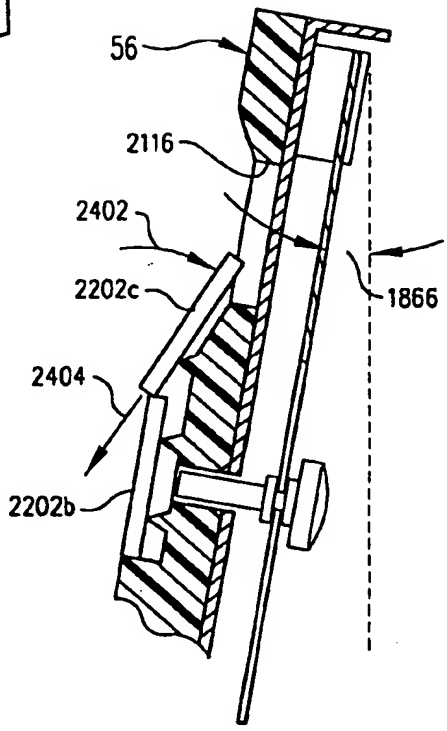


Fig. 24

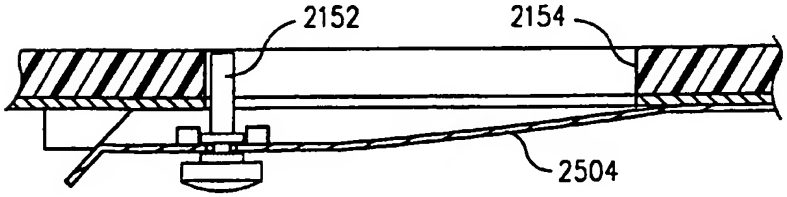
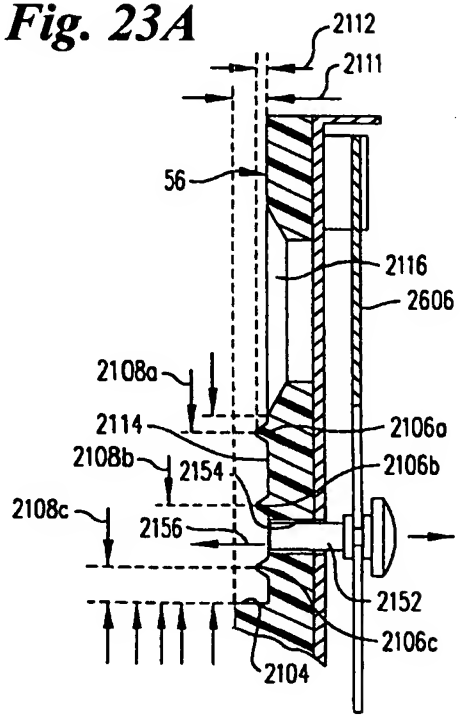


Fig. 26

Fig. 23A



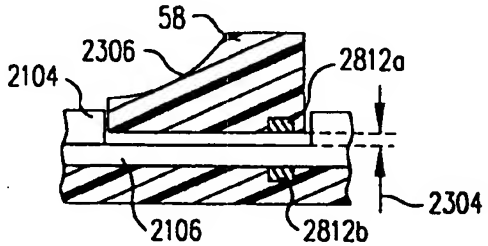


Fig. 23D

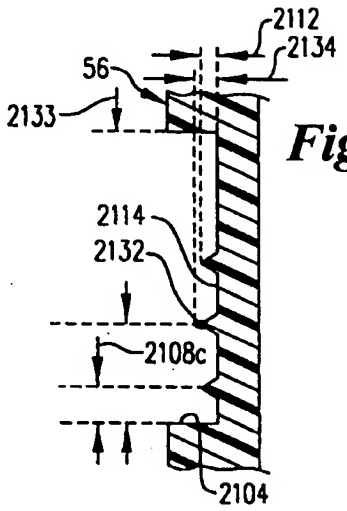


Fig. 23B

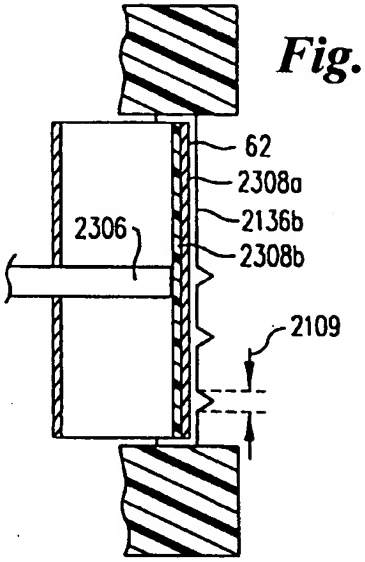


Fig. 23C

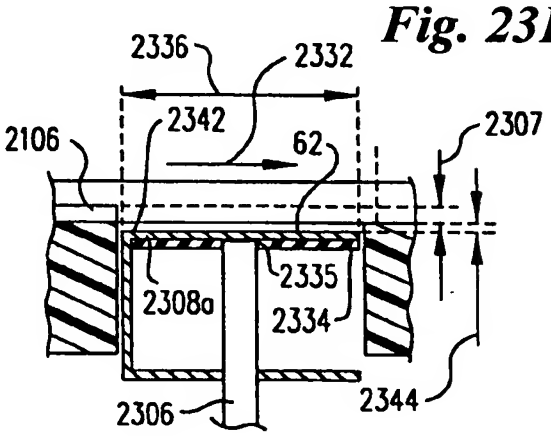


Fig. 23E

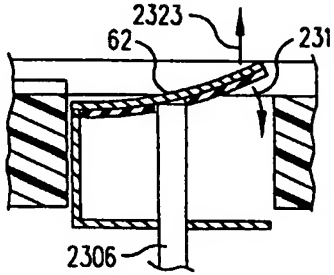


Fig. 23F

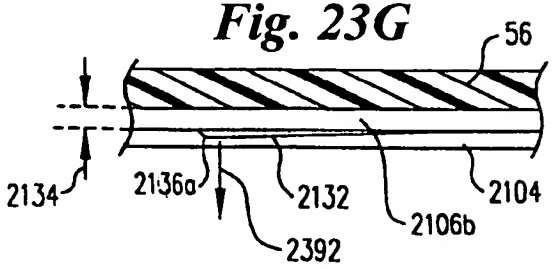


Fig. 23G

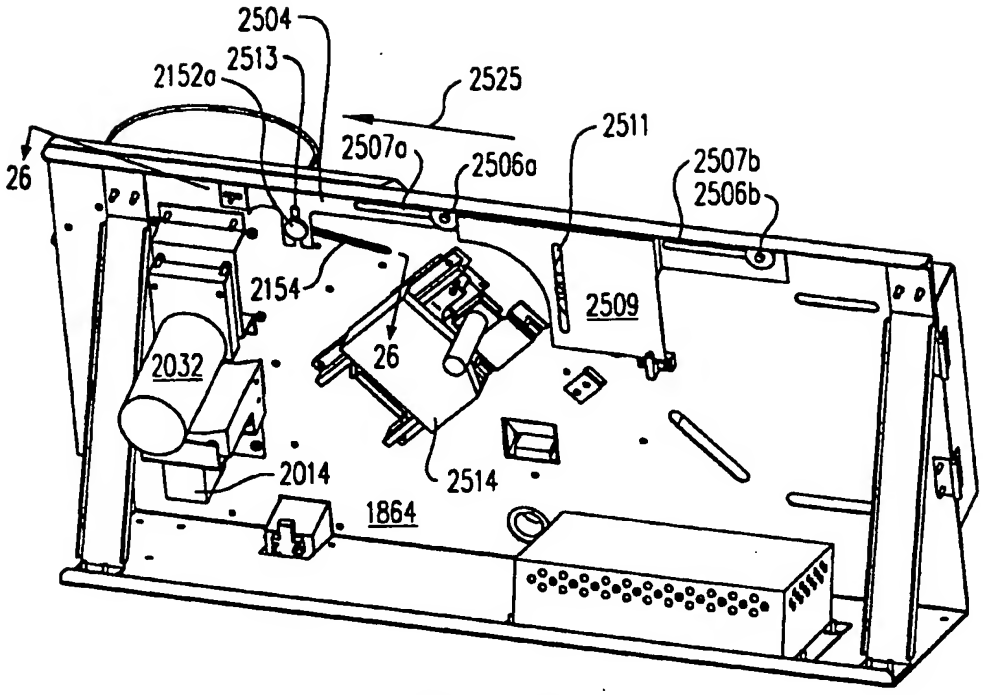


Fig. 25

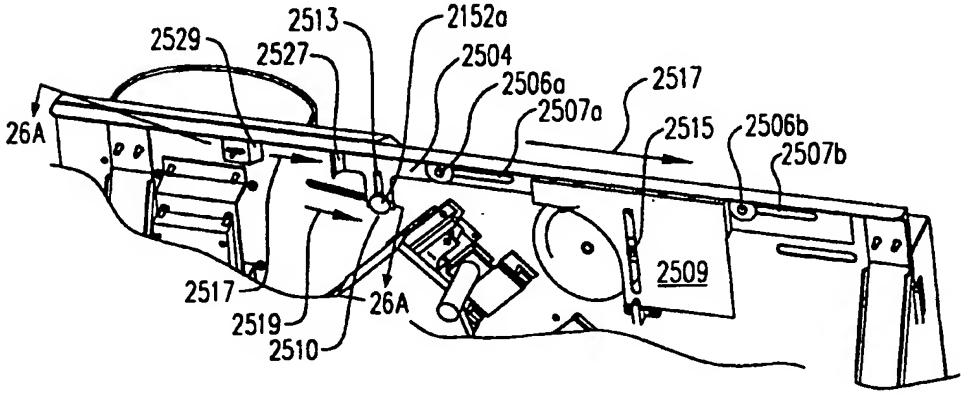


Fig. 25A

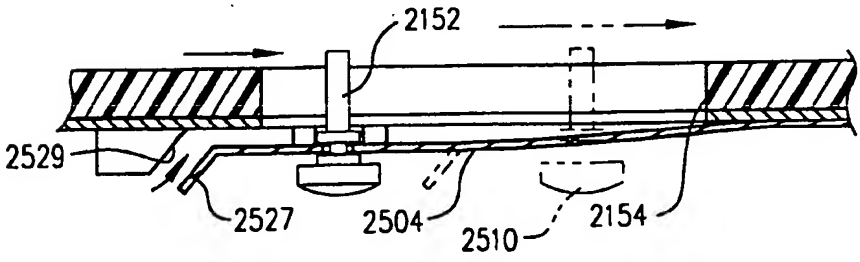


Fig. 26A

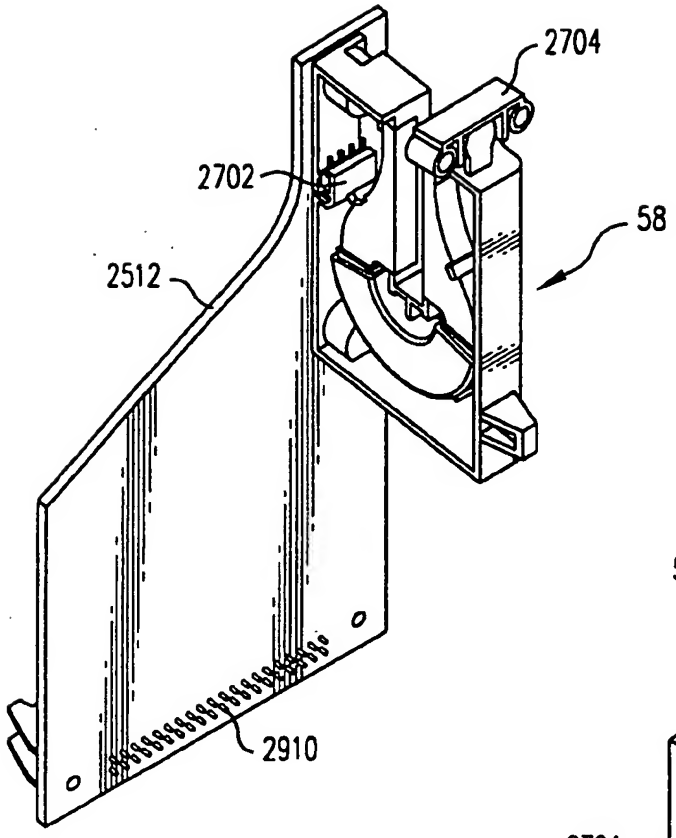


Fig. 27A

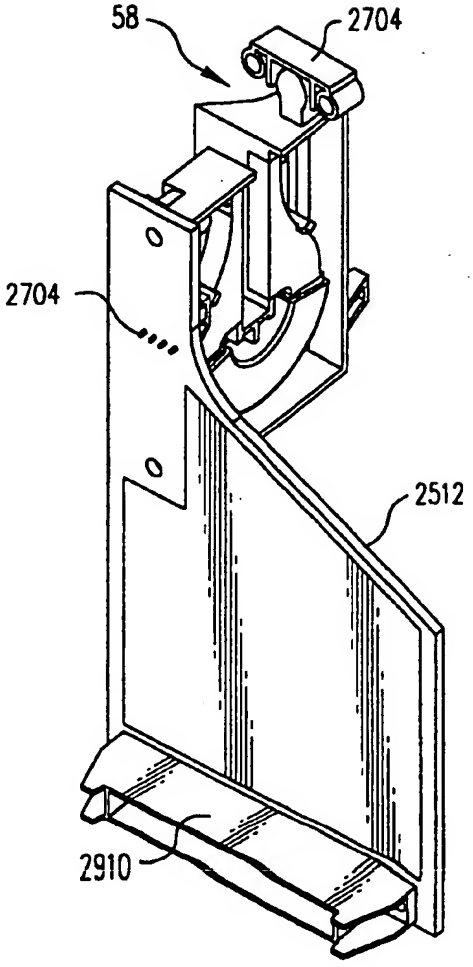


Fig. 27B

FIG. 29A	FIG. 29B

Fig. 29

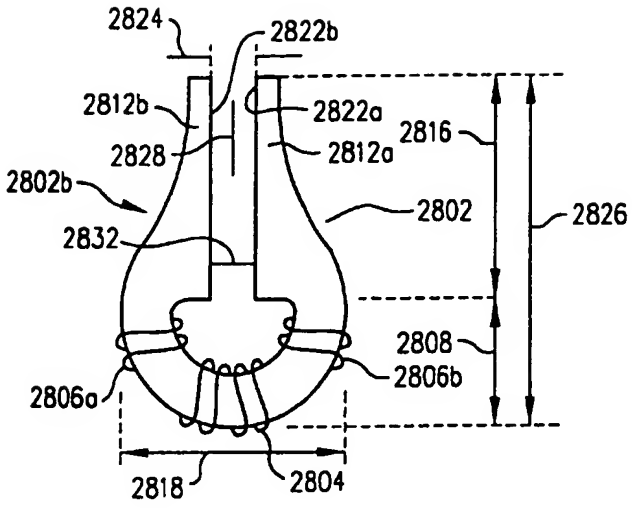


Fig. 28A

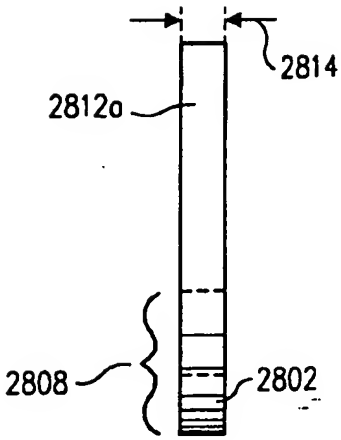
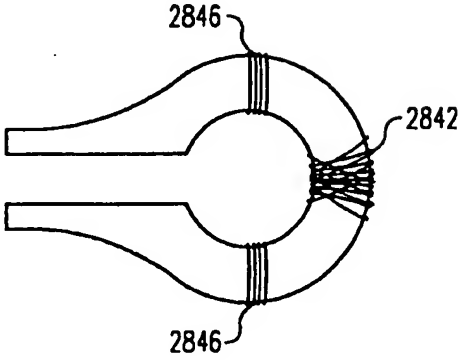


Fig. 28B

Fig. 28C



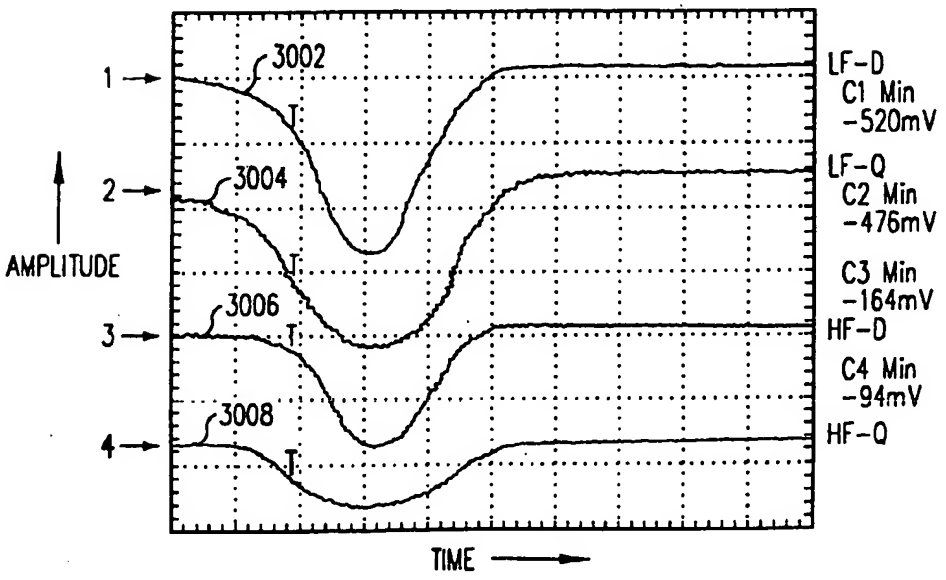


Fig. 30

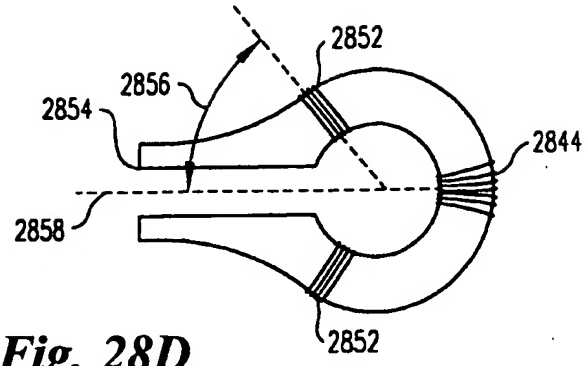


Fig. 28D

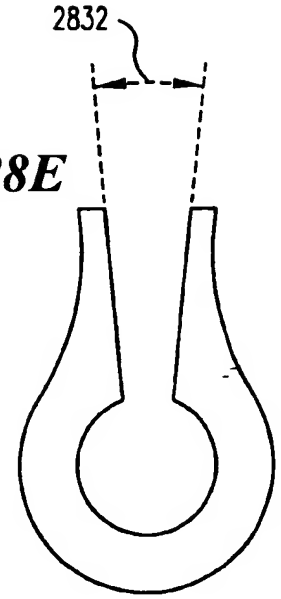


Fig. 28E

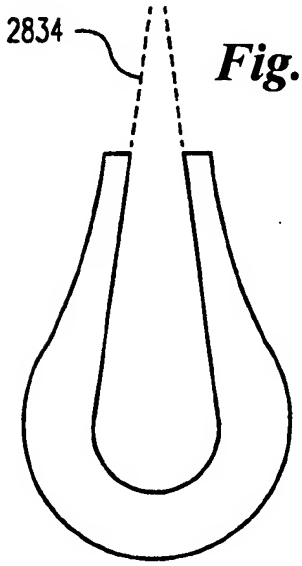


Fig. 28F

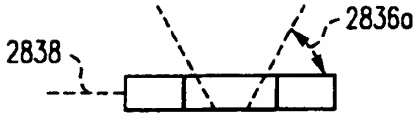


Fig. 28G

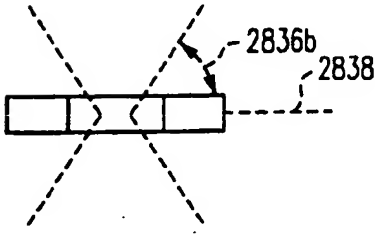


Fig. 28H

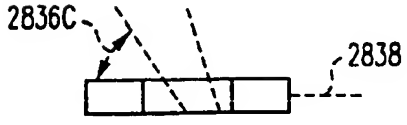


Fig. 28I

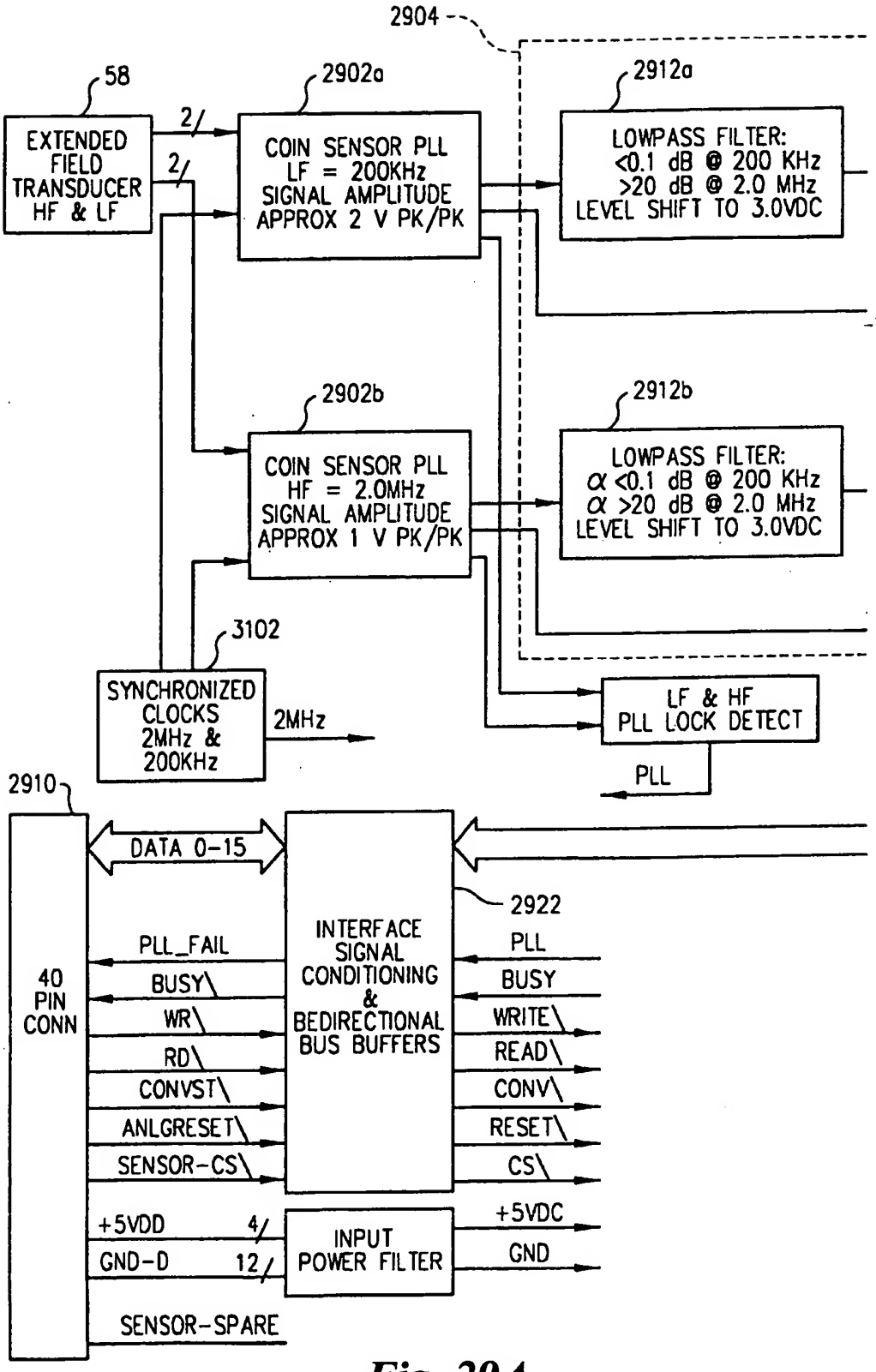

2904
58
EXTENDED FIELD TRANSDUCER HF & LF
2
2
2902a
COIN SENSOR PLL
LF = 200KHz
SIGNAL AMPLITUDE
APPROX 2 V PK/PK
2912a
LOWPASS FILTER:
<0.1 dB @ 200 KHz
>20 dB @ 2.0 MHz
LEVEL SHIFT TO 3.0VDC
2902b
COIN SENSOR PLL
HF = 2.0MHz
SIGNAL AMPLITUDE
APPROX 1 V PK/PK
2912b
LOWPASS FILTER:
α <0.1 dB @ 200 KHz
α >20 dB @ 2.0 MHz
LEVEL SHIFT TO 3.0VDC
3102
SYNCHRONIZED CLOCKS
2MHz &
200KHz
2MHz
LF & HF
PLL LOCK DETECT
PLL
2910
DATA 0-15
2922
40 PIN CONN
INTERFACE SIGNAL CONDITIONING & BEDIRECTIONAL BUS BUFFERS
PLL_FAIL
BUSY\
WR\
RD\
CONVST\
ANLGRESET\
SENSOR-CS\
PLL
BUSY
WRITE\
READ\
CONV\
RESET\
CS\
+5VDD
4
GND-D
12
INPUT POWER FILTER
+5VDC
GND
SENSOR-SPARE

Fig. 29A

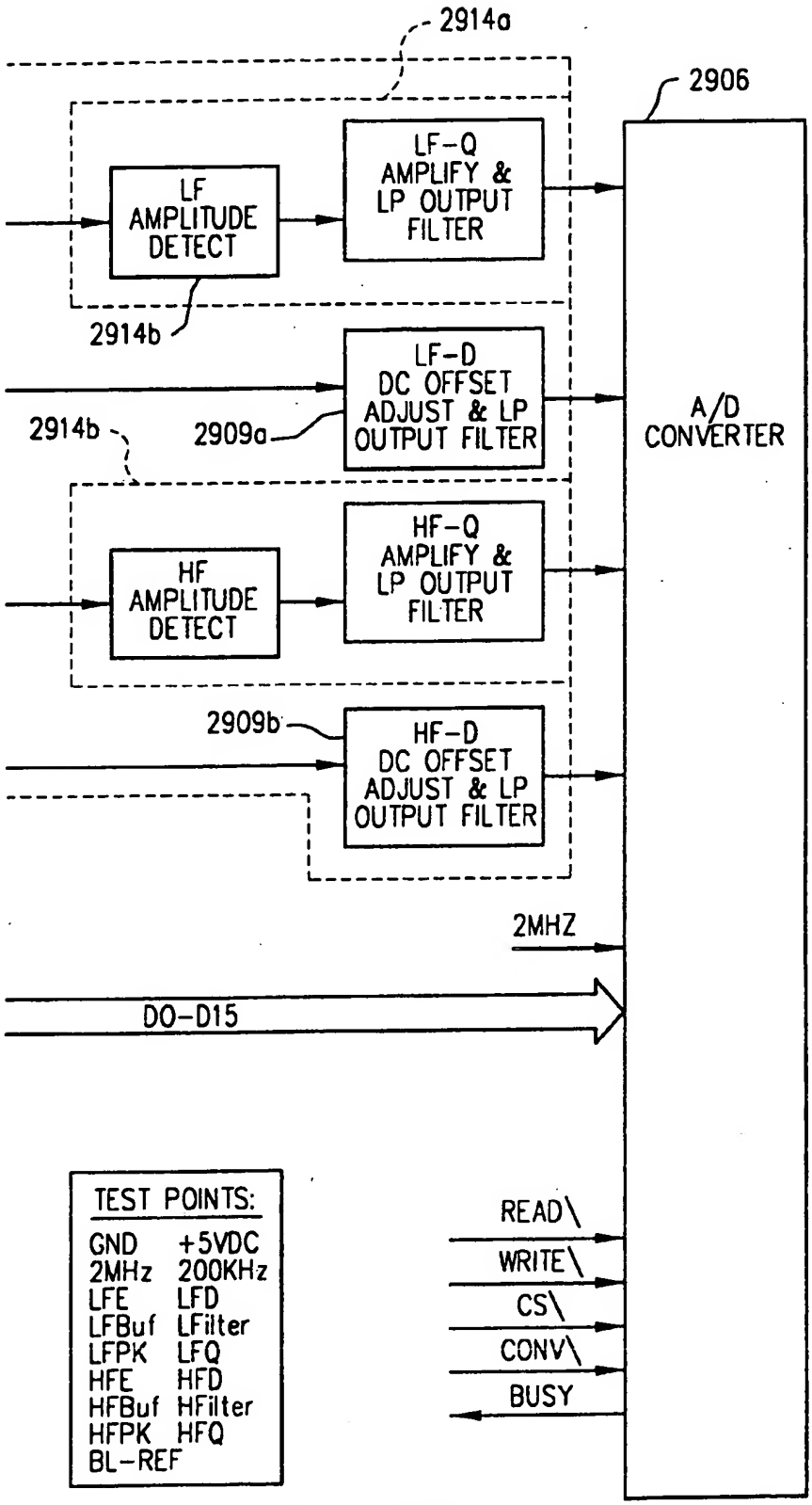

2914a
2906
LF
AMPLITUDE
DETECT
LF-Q
AMPLIFY &
LP OUTPUT
FILTER
2914b
LF-D
DC OFFSET
ADJUST & LP
OUTPUT FILTER
2914b
2909a
A/D
CONVERTER
HF
AMPLITUDE
DETECT
HF-Q
AMPLIFY &
LP OUTPUT
FILTER
2909b
HF-D
DC OFFSET
ADJUST & LP
OUTPUT FILTER
2MHZ
D0-D15
TEST POINTS:
GND +5VDC
2MHz 200KHz
LFE LFD
LFBuf LFilter
LFPK LFQ
HFE HFD
HFBuf HFilter
HFPK HFQ
BL-REF
READ\
WRITE\
CS\
CONV\
BUSY

Fig. 29B

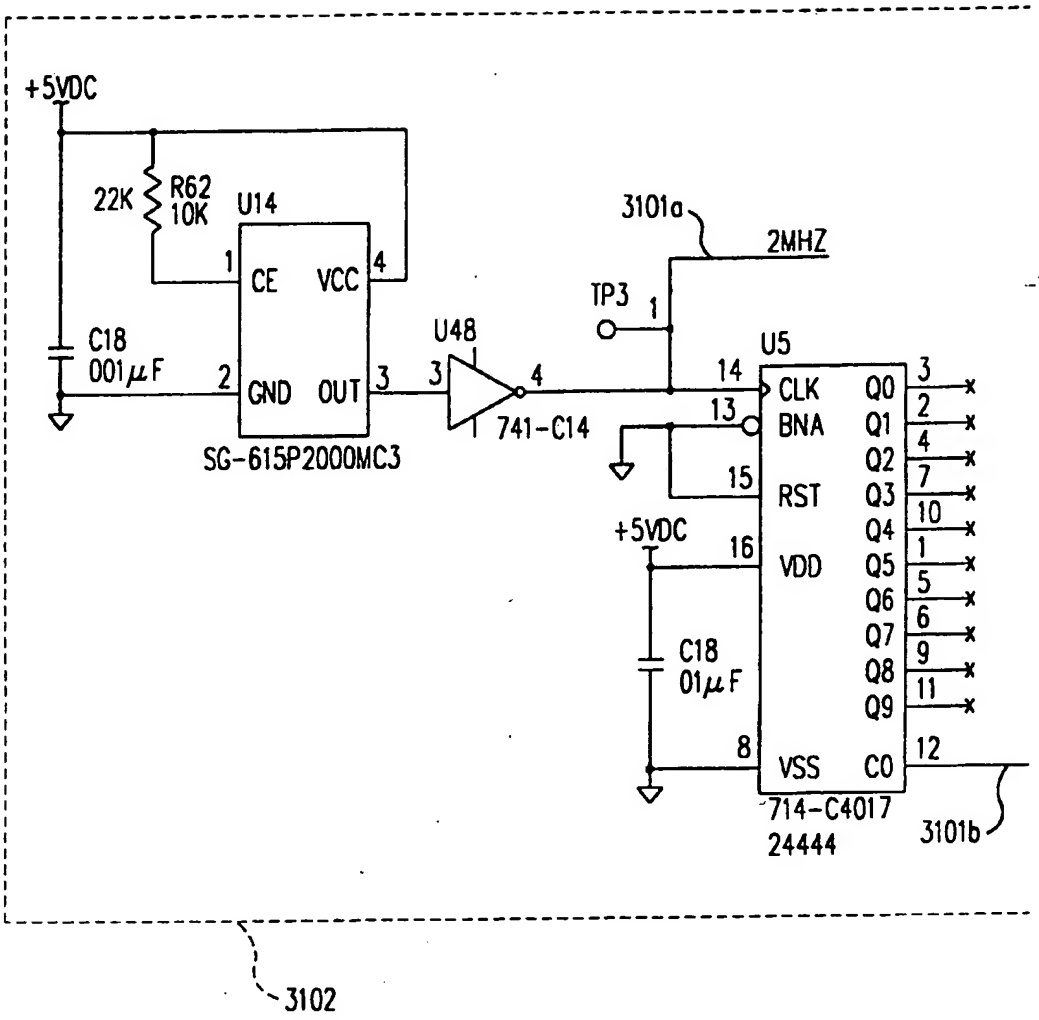

+5VDC
22K
R62
10K
U14
1
CE
VCC
4
C18
001μF
2
GND
OUT
3
SG-615P2000MC3
3
U48
4
741-C14
3101a
2MHZ
TP3
1
U5
14
CLK
13
BNA
15
RST
+5VDC
16
VDD
C18
01μF
8
VSS
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
C0
3
2
4
7
10
1
5
6
9
11
12
714-C4017
24444
3101b
3102

Fig. 31A

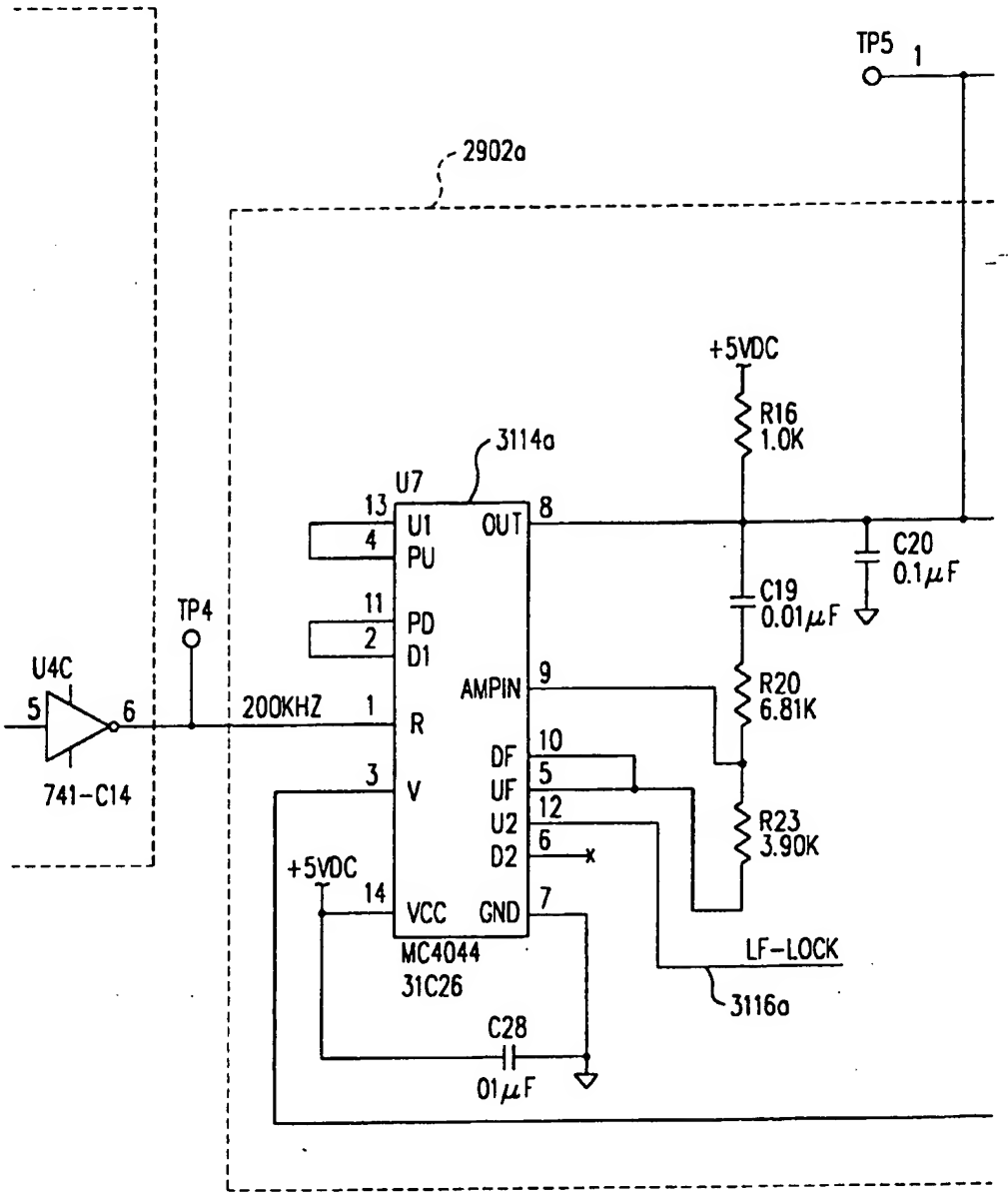

TP5
1
2902a
+5VDC
R16
1.0K
3114a
U7
13
U1
4
PU
11
PD
2
D1
OUT
8
C20
0.1μF
C19
0.01μF
TP4
U4C
5
6
741-C14
200KHZ
1
R
AMPIN
9
R20
6.81K
DF
10
3
V
UF
5
U2
12
D2
6
R23
3.90K
+5VDC
14
VCC
GND
7
MC4044
31C26
LF-LOCK
3116a
C28
01μF

Fig. 31B

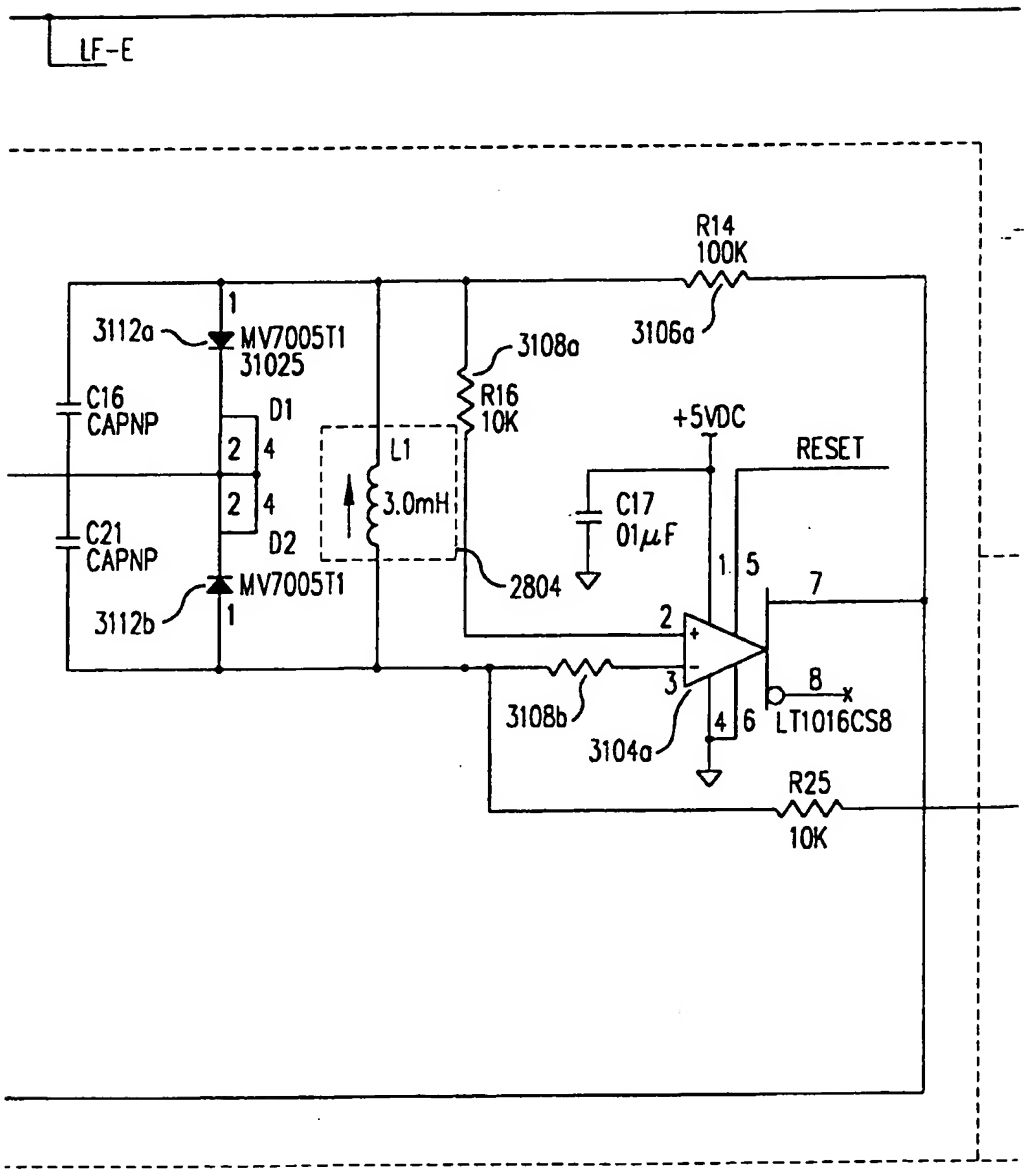

LF-E
R14
100K
3106a
3112a
MV7005T1
31025
3108a
R16
10K
C16
CAPNP
D1
L1
3.0mH
+5VDC
RESET
C17
01μF
C21
CAPNP
D2
MV7005T1
3112b
2804
3108b
3104a
LT1016CS8
R25
10K

Fig. 31C

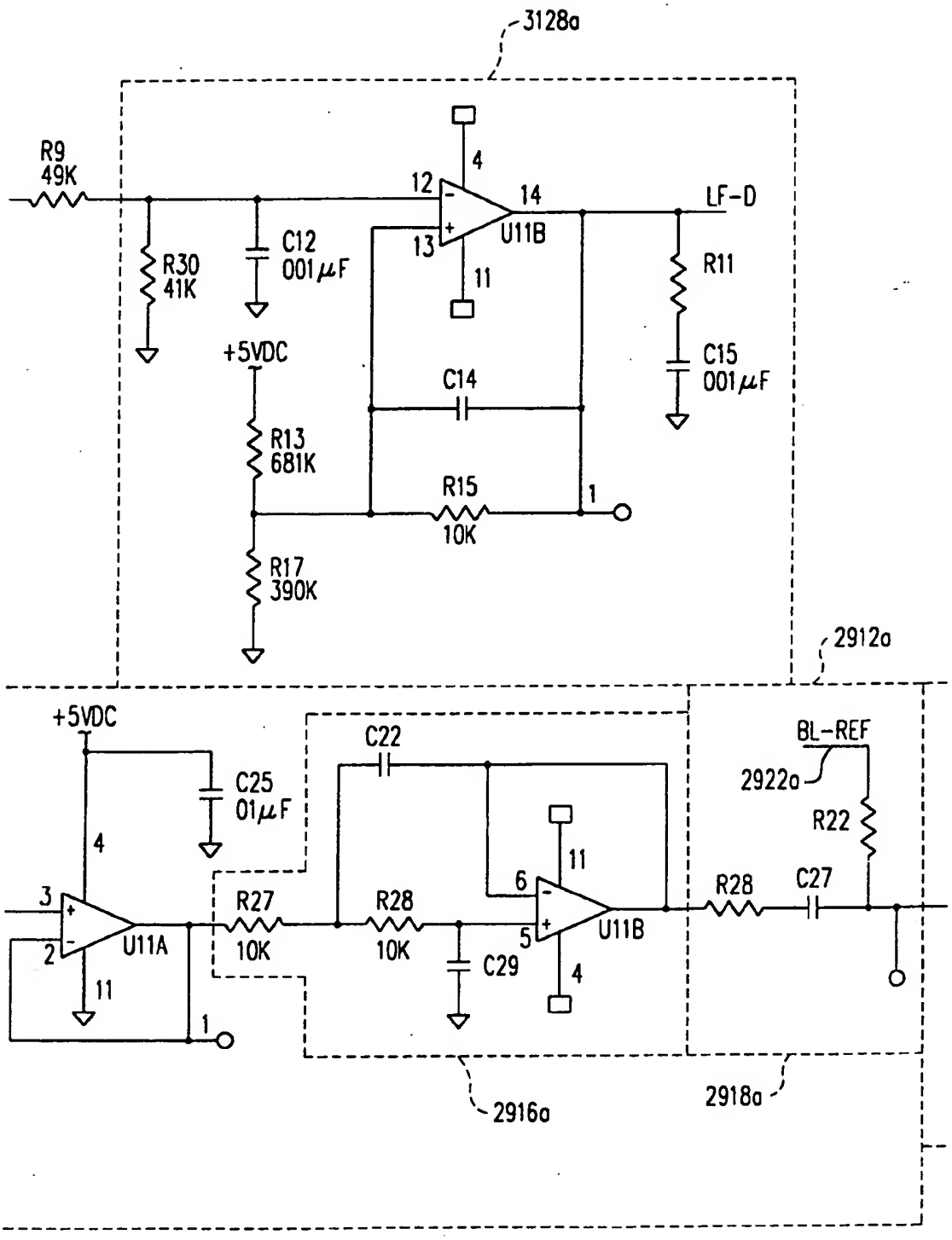

3128a
R9
49K
12
4
14
LF-D
13
U11B
11
R30
41K
C12
001μF
R11
C15
001μF
+5VDC
C14
R13
681K
R15
10K
1
R17
390K
2912a
+5VDC
C22
BL-REF
2922a
C25
01μF
R22
4
11
6
3
R27
R28
R28
C27
10K
10K
U11B
5
U11A
2
C29
4
11
1
2916a
2918a

Fig. 31D

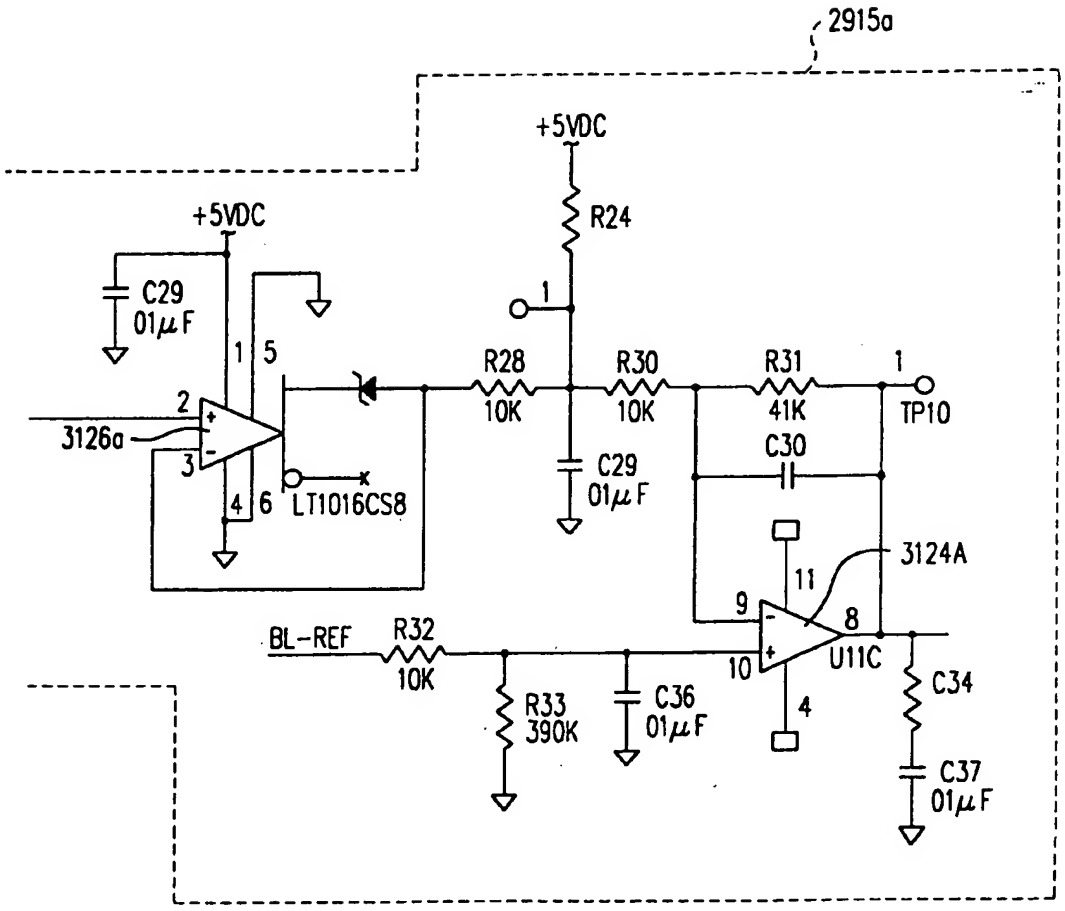

2915a
+5VDC
R24
+5VDC
C29
01μF
1
5
R28
10K
R30
10K
R31
41K
1
TP10
2
3126a
3
4
6
LT1016CS8
C30
C29
01μF
3124A
11
9
8
BL-REF
R32
10K
10
U11C
C34
R33
390K
C36
01μF
4
C37
01μF

Fig. 31E

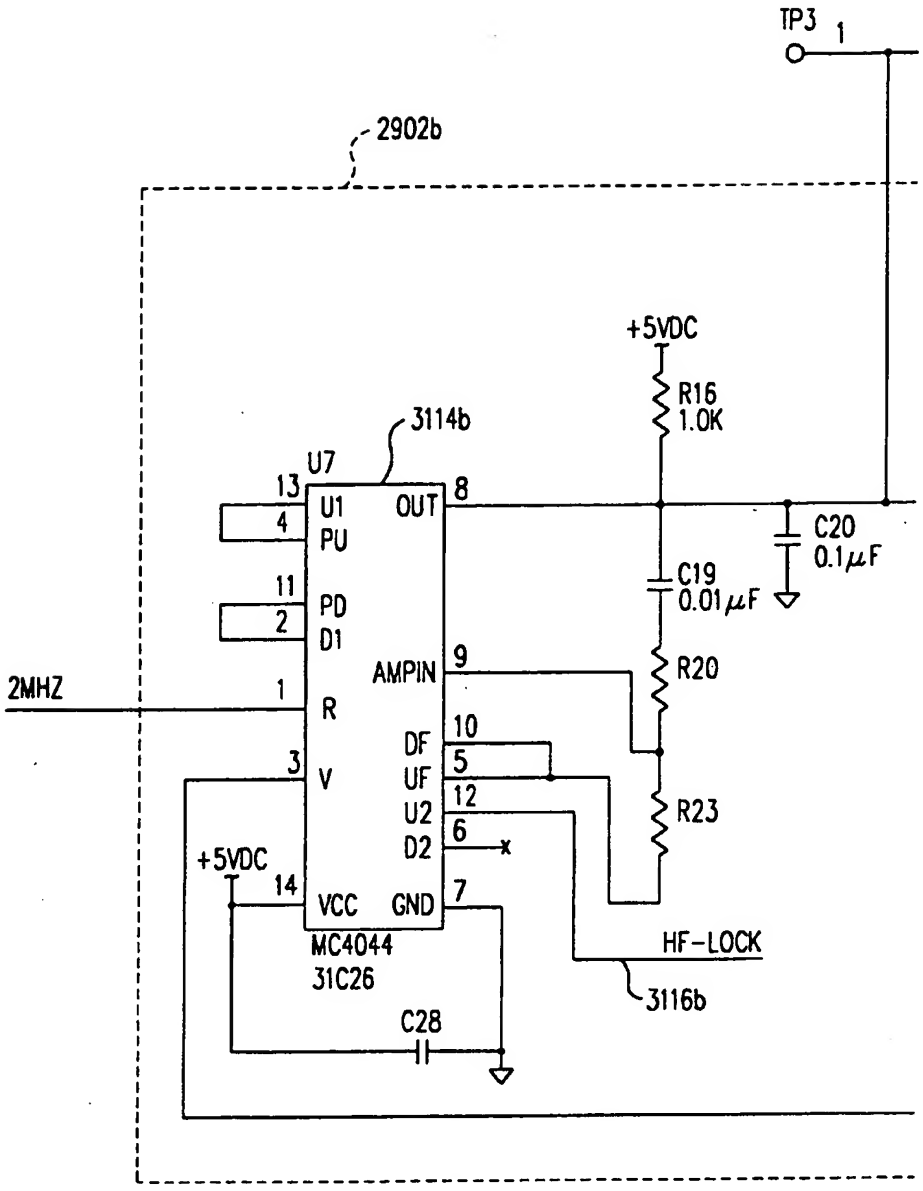

TP3
1
2902b
+5VDC
R16
1.0K
3114b
U7
13
U1
4
PU
11
PD
2
D1
2MHZ
1
R
3
V
14
VCC
MC4044
31C26
OUT
8
C20
0.1μF
C19
0.01μF
AMPIN
9
R20
DF
10
UF
5
U2
12
D2
6
R23
GND
7
HF-LOCK
3116b
C28

Fig. 31F

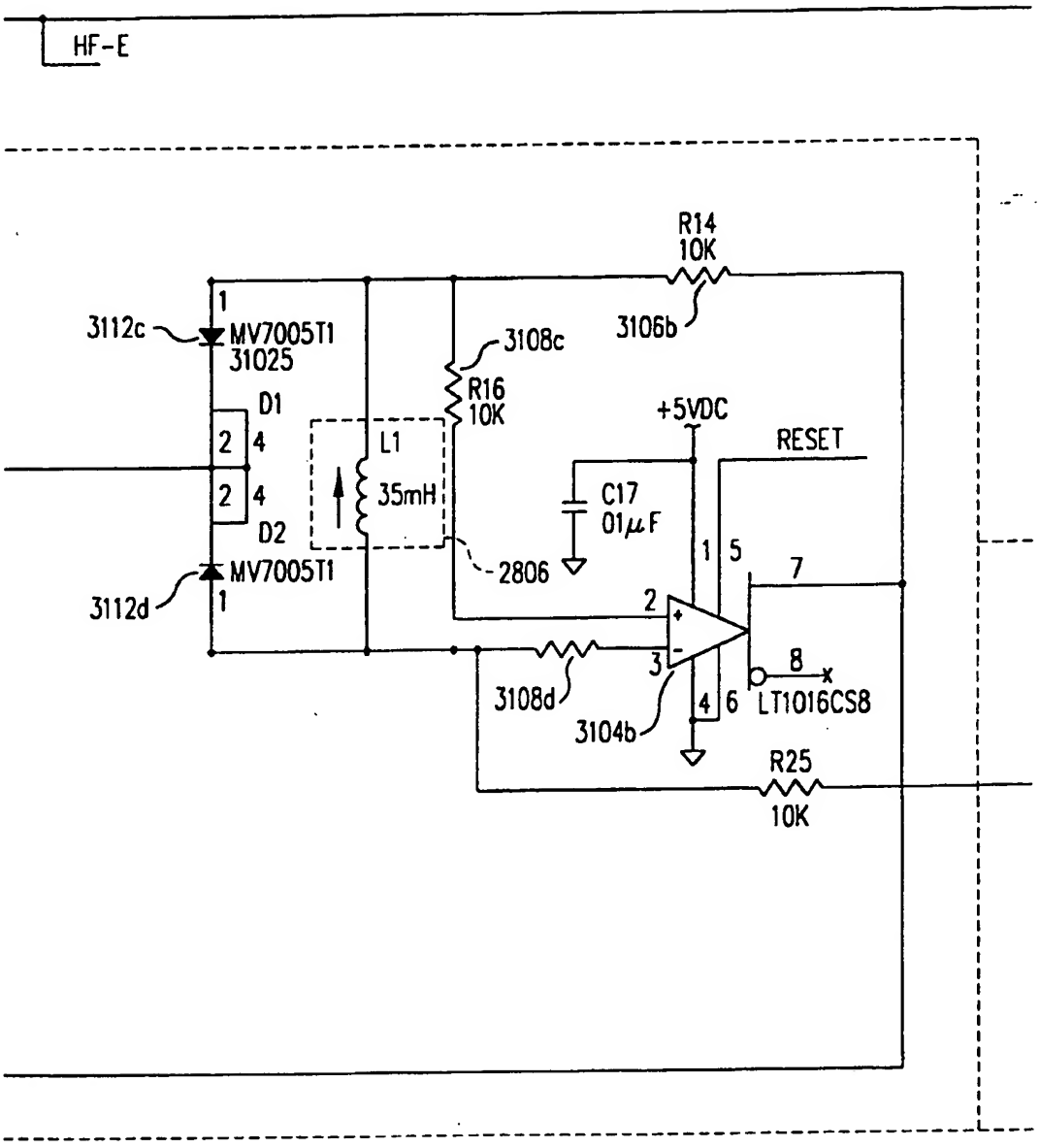

HF-E
R14
10K
3106b
3112c
MV7005T1
31025
3108c
R16
10K
D1
2
4
2
4
D2
L1
35mH
+5VDC
RESET
C17
01μF
2806
1
5
7
3112d
MV7005T1
1
2
3
8
x
3108d
3104b
4
6
LT1016CS8
R25
10K

Fig. 31G

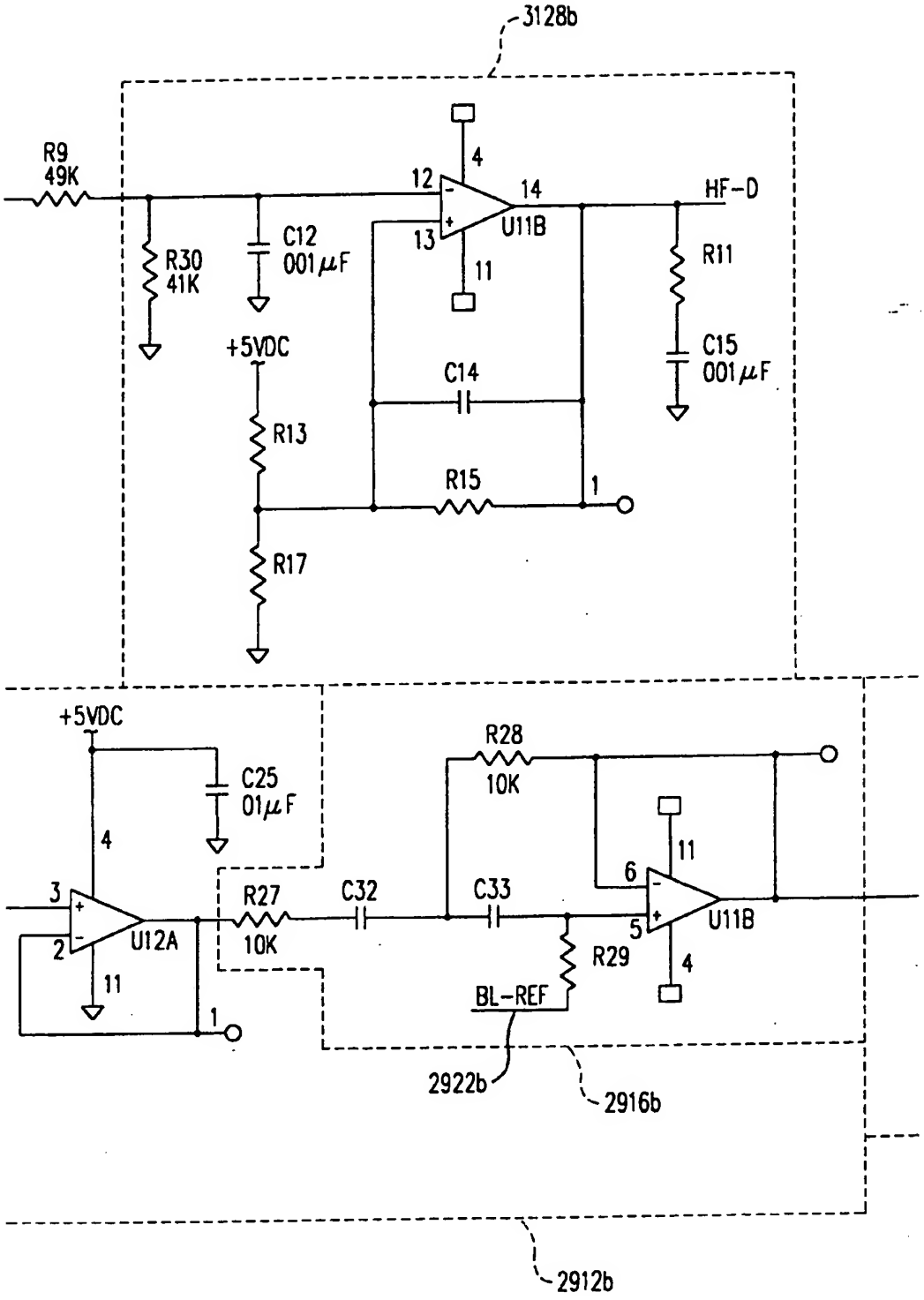

3128b
R9
49K
R30
41K
C12
001μF
12
13
4
11
14
U11B
HF-D
R11
C15
001μF
+5VDC
C14
R13
R15
1
R17
+5VDC
C25
01μF
4
3
2
U12A
11
1
R27
10K
C32
C33
R28
10K
6
5
11
U11B
4
R29
BL-REF
2922b
2916b
2912b

Fig. 31H

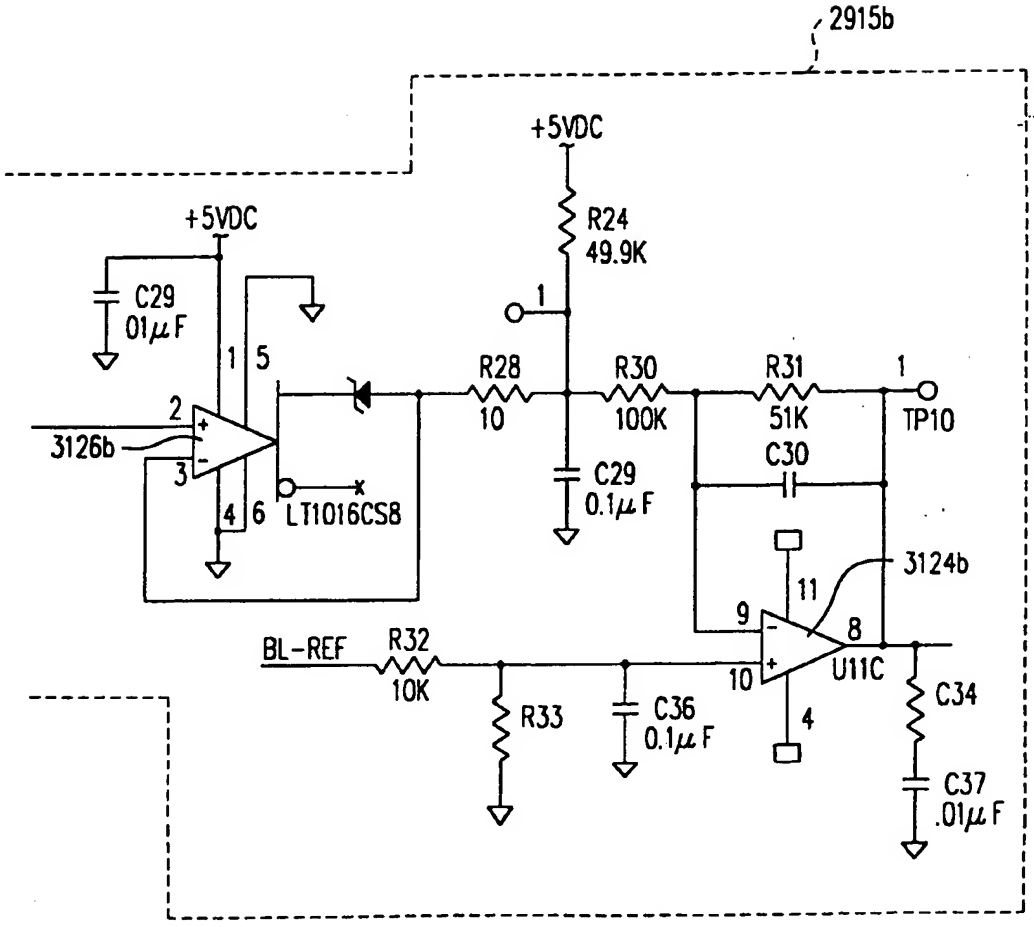

2915b
+5VDC
R24
49.9K
+5VDC
C29
01μF
1
5
R28
10
R30
100K
R31
51K
1
TP10
2
3126b
3
4
6
LT1016CS8
C29
0.1μF
C30
3124b
11
9
8
BL-REF
R32
10K
10
U11C
4
R33
C36
0.1μF
C34
C37
.01μF

Fig. 31I

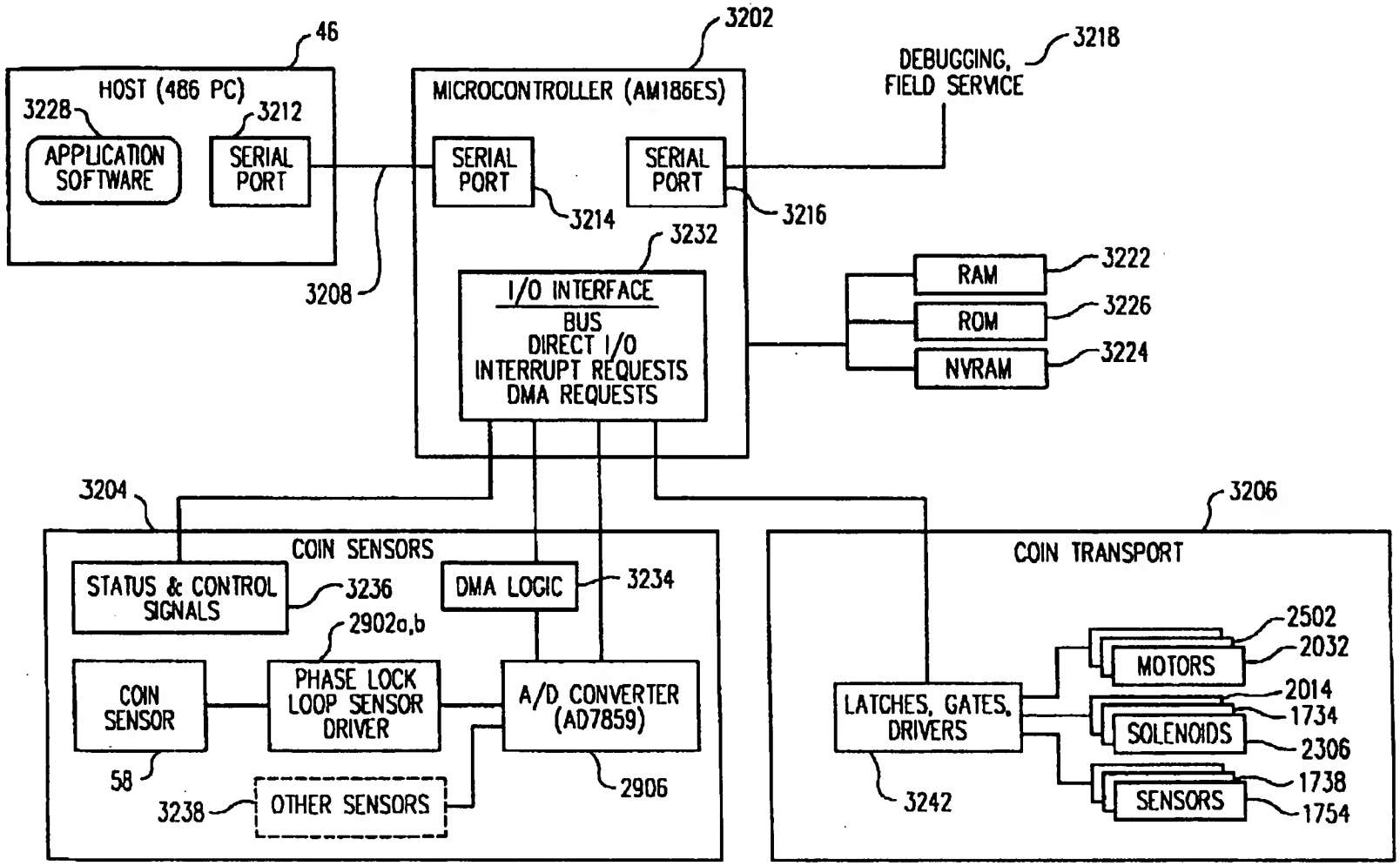

46
HOST (486 PC)
3228
APPLICATION SOFTWARE
3212
SERIAL PORT
3208
3202
MICROCONTROLLER (AM186ES)
SERIAL PORT
3214
SERIAL PORT
3216
DEBUGGING, FIELD SERVICE
3218
3232
I/O INTERFACE
BUS
DIRECT I/O
INTERRUPT REQUESTS
DMA REQUESTS
RAM
3222
ROM
3226
NVRAM
3224
3204
COIN SENSORS
STATUS & CONTROL SIGNALS
3236
DMA LOGIC
3234
2902a,b
COIN SENSOR
PHASE LOCK LOOP SENSOR DRIVER
A/D CONVERTER (AD7859)
58
3238
OTHER SENSORS
2906
3206
COIN TRANSPORT
LATCHES, GATES, DRIVERS
3242
MOTORS
2502
2032
SOLENOIDS
2014
1734
2306
SENSORS
1738
1754

Fig. 32

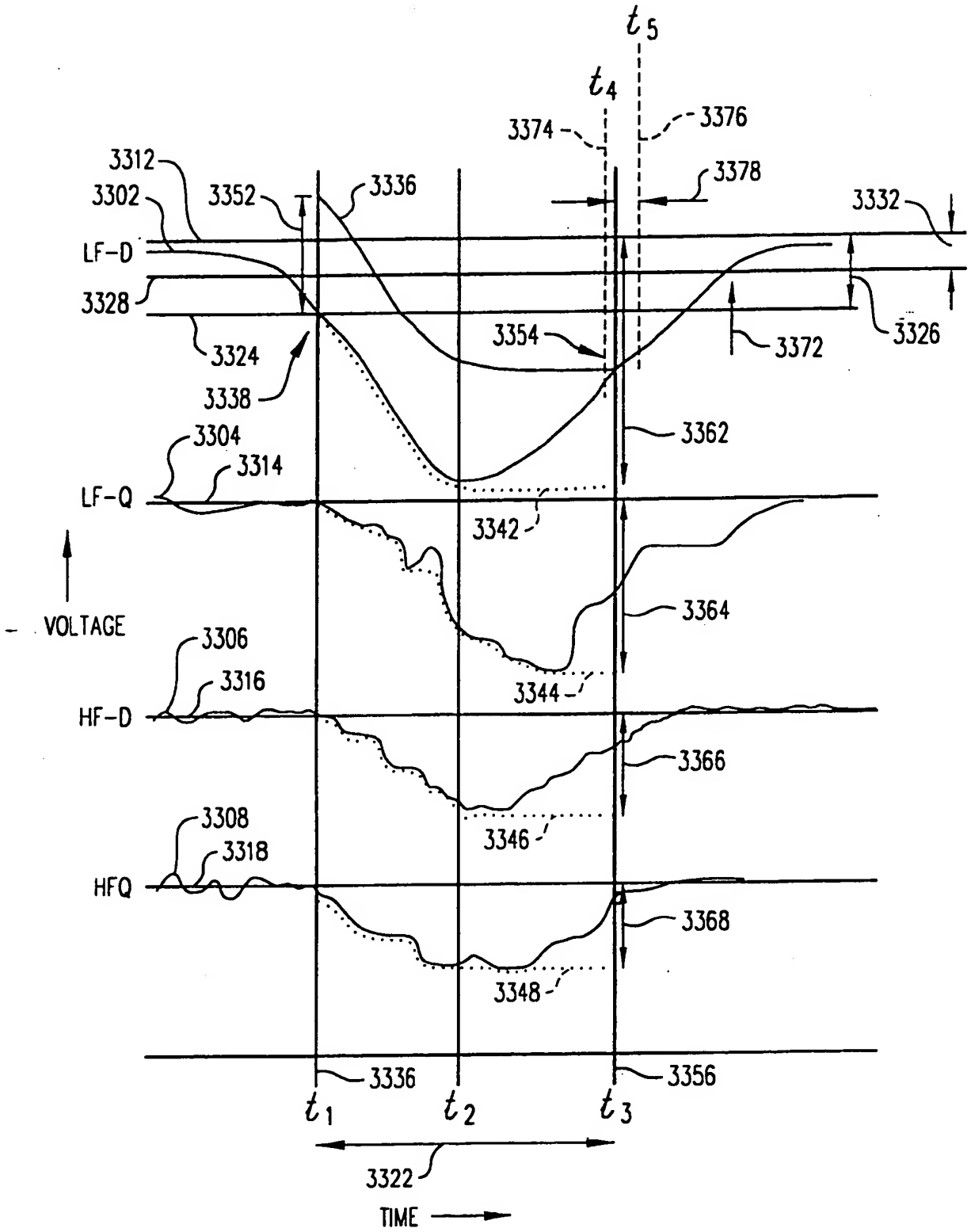

t_5
t_4
3374
3376
3312
3378
3302
3352
3336
3332
LF-D
3328
3354
3372
3326
3324
3338
3362
3304
3314
LF-Q
3342
VOLTAGE
3364
3306
3316
3344
HF-D
3366
3308
3346
3318
HFQ
3368
3348
3336
3356
t_1
t_2
t_3
3322
TIME

Fig. 33

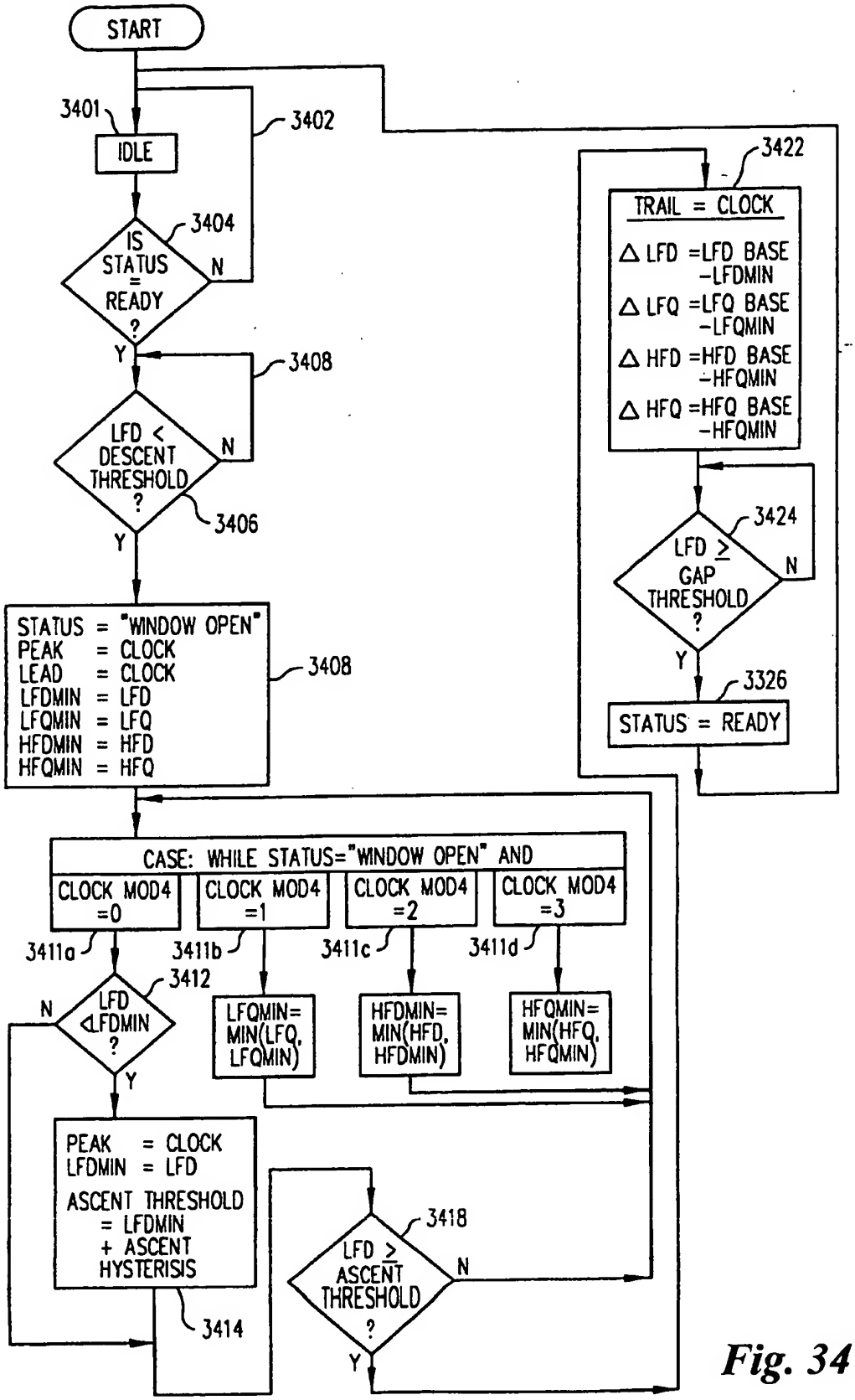

START
3401
IDLE
3402
3404
IS STATUS = READY ?
N
Y
3408
LFD < DESCENT THRESHOLD ?
N
3406
Y
STATUS = "WINDOW OPEN"
PEAK = CLOCK
LEAD = CLOCK
LFDMIN = LFD
LFQMIN = LFQ
HFDMIN = HFD
HFQMIN = HFQ
3408
3422
TRAIL = CLOCK
Δ LFD =LFD BASE -LFDMIN
Δ LFQ =LFQ BASE -LFQMIN
Δ HFD =HFD BASE -HFQMIN
Δ HFQ =HFQ BASE -HFQMIN
3424
LFD ≥ GAP THRESHOLD ?
N
Y
3326
STATUS = READY
CASE: WHILE STATUS="WINDOW OPEN" AND
CLOCK MOD4 =0
CLOCK MOD4 =1
CLOCK MOD4 =2
CLOCK MOD4 =3
3411a
3411b
3411c
3411d
3412
LFD <LFDMIN ?
N
Y
LFQMIN= MIN(LFQ, LFQMIN)
HFDMIN= MIN(HFD, HFDMIN)
HFQMIN= MIN(HFQ, HFQMIN)
PEAK = CLOCK
LFDMIN = LFD
ASCENT THRESHOLD = LFDMIN + ASCENT HYSTERISIS
3414
3418
LFD ≥ ASCENT THRESHOLD ?
N
Y

Fig. 34

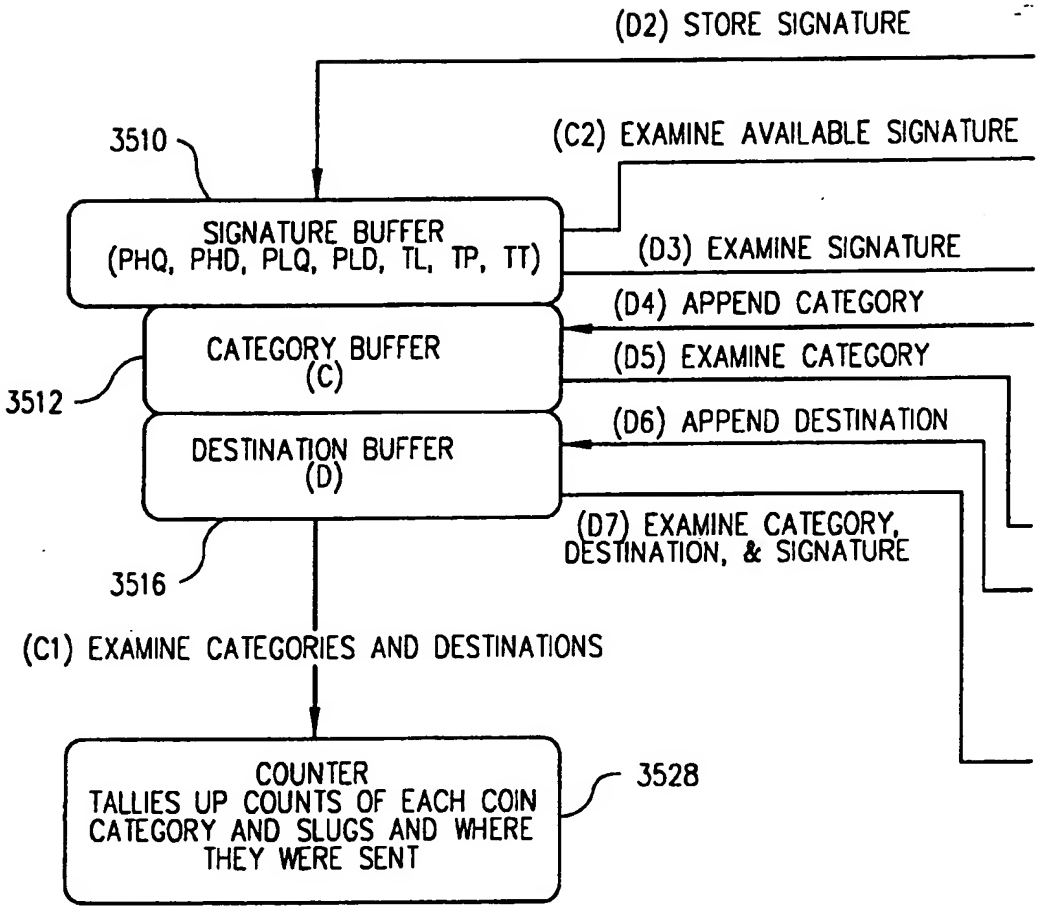

(D2) STORE SIGNATURE
3510
(C2) EXAMINE AVAILABLE SIGNATURE
SIGNATURE BUFFER
(PHQ, PHD, PLQ, PLD, TL, TP, TT)
(D3) EXAMINE SIGNATURE
(D4) APPEND CATEGORY
CATEGORY BUFFER
(C)
(D5) EXAMINE CATEGORY
3512
(D6) APPEND DESTINATION
DESTINATION BUFFER
(D)
(D7) EXAMINE CATEGORY,
DESTINATION, & SIGNATURE
3516
(C1) EXAMINE CATEGORIES AND DESTINATIONS
COUNTER
TALLIES UP COUNTS OF EACH COIN
CATEGORY AND SLUGS AND WHERE
THEY WERE SENT
3528

Fig. 35A

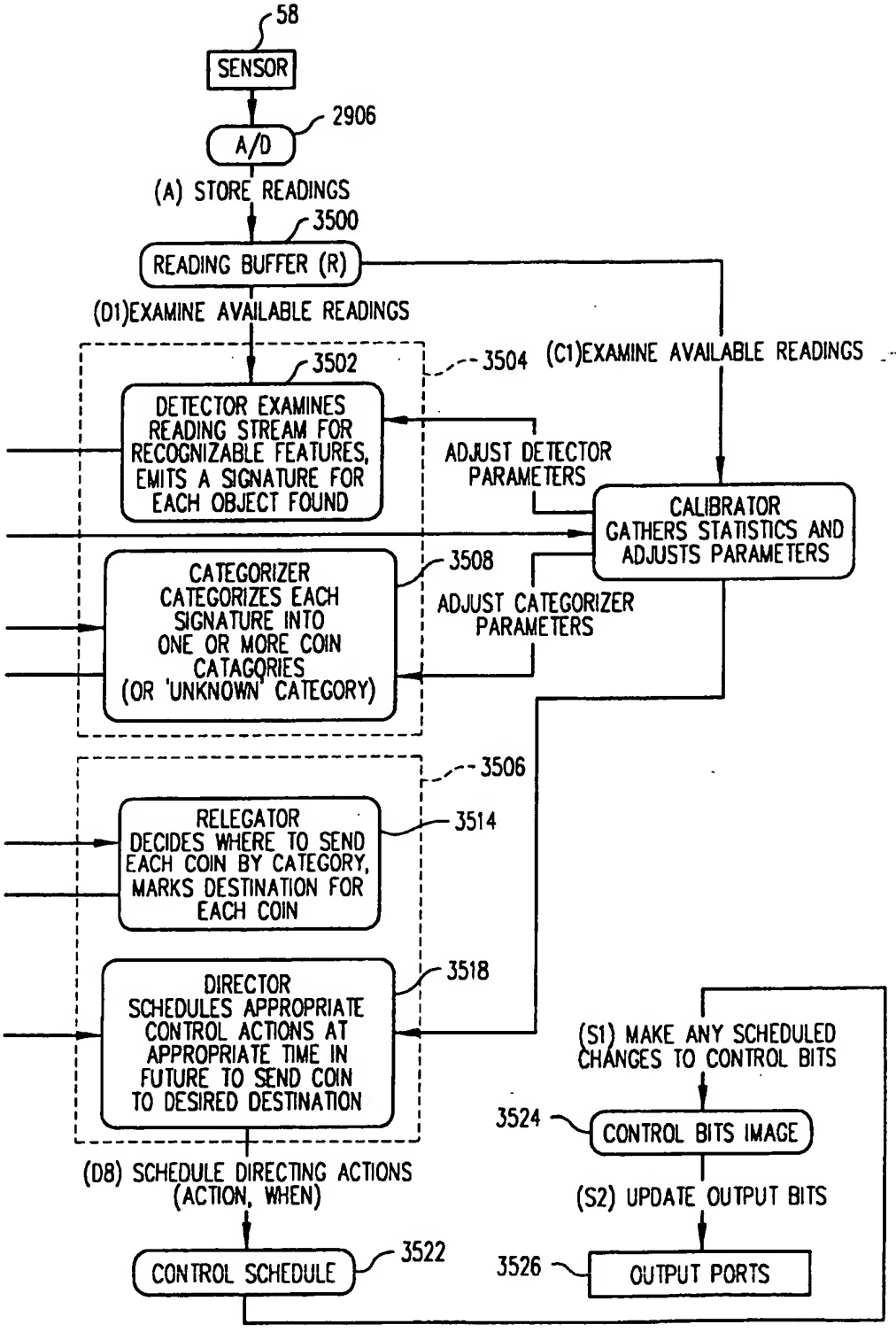

58
SENSOR
2906
A/D
(A) STORE READINGS
3500
READING BUFFER (R)
(D1)EXAMINE AVAILABLE READINGS
3504
(C1)EXAMINE AVAILABLE READINGS
3502
DETECTOR EXAMINES READING STREAM FOR RECOGNIZABLE FEATURES, EMITS A SIGNATURE FOR EACH OBJECT FOUND
ADJUST DETECTOR PARAMETERS
CALIBRATOR GATHERS STATISTICS AND ADJUSTS PARAMETERS
3508
CATEGORIZER CATEGORIZES EACH SIGNATURE INTO ONE OR MORE COIN CATAGORIES (OR 'UNKNOWN' CATEGORY)
ADJUST CATEGORIZER PARAMETERS
3506
RELEGATOR DECIDES WHERE TO SEND EACH COIN BY CATEGORY, MARKS DESTINATION FOR EACH COIN
3514
DIRECTOR SCHEDULES APPROPRIATE CONTROL ACTIONS AT APPROPRIATE TIME IN FUTURE TO SEND COIN TO DESIRED DESTINATION
3518
(S1) MAKE ANY SCHEDULED CHANGES TO CONTROL BITS
3524
CONTROL BITS IMAGE
(S2) UPDATE OUTPUT BITS
(D8) SCHEDULE DIRECTING ACTIONS (ACTION, WHEN)
CONTROL SCHEDULE
3522
3526
OUTPUT PORTS

Fig. 35B

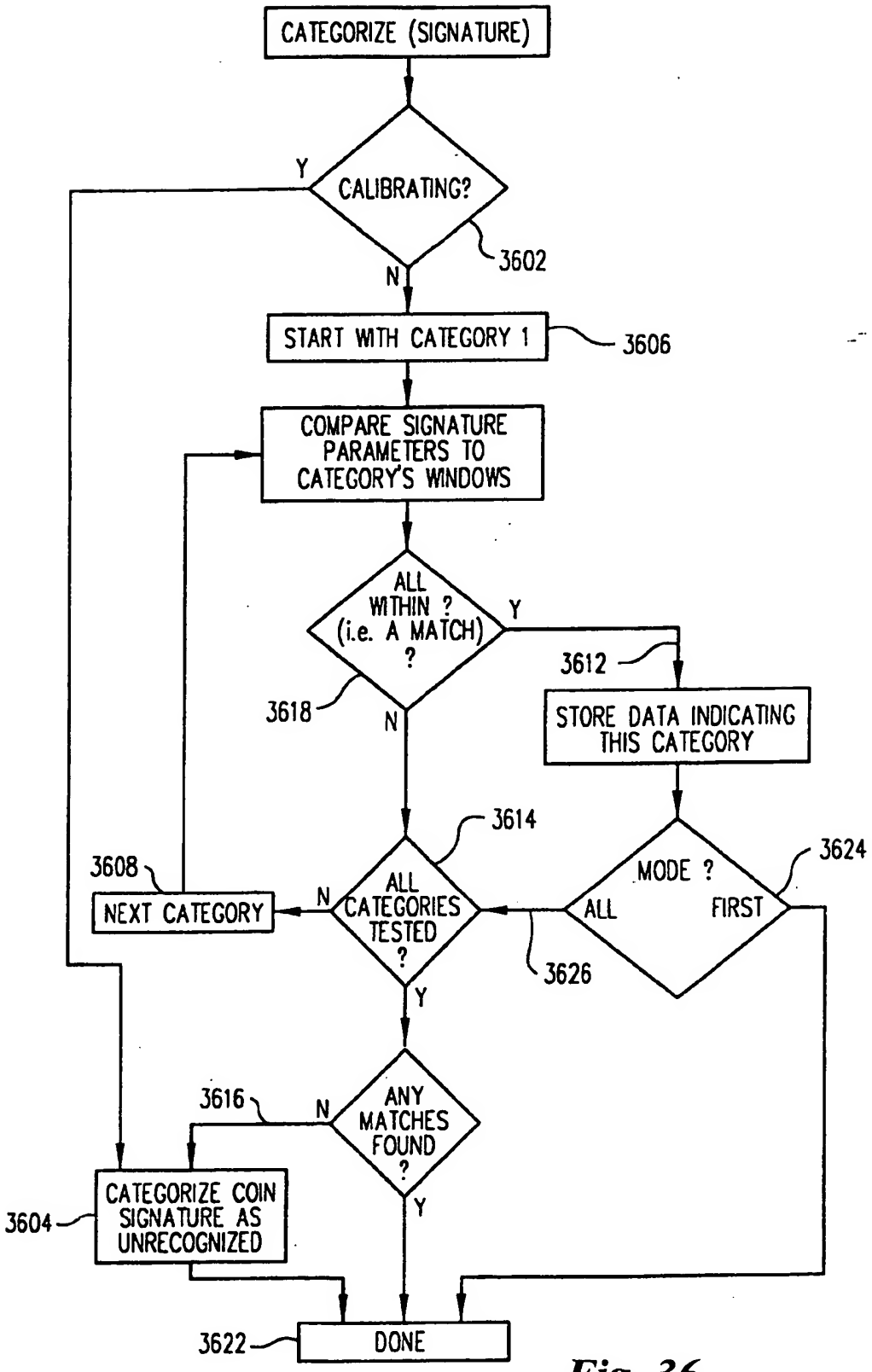

CATEGORIZE (SIGNATURE)
CALIBRATING?
Y
N
3602
START WITH CATEGORY 1
3606
COMPARE SIGNATURE PARAMETERS TO CATEGORY'S WINDOWS
ALL WITHIN ? (i.e. A MATCH) ?
Y
N
3618
3612
STORE DATA INDICATING THIS CATEGORY
3614
MODE ?
ALL
FIRST
3624
3626
ALL CATEGORIES TESTED ?
N
Y
3608
NEXT CATEGORY
3616
ANY MATCHES FOUND ?
N
Y
CATEGORIZE COIN SIGNATURE AS UNRECOGNIZED
3604
3622
DONE

Fig. 36

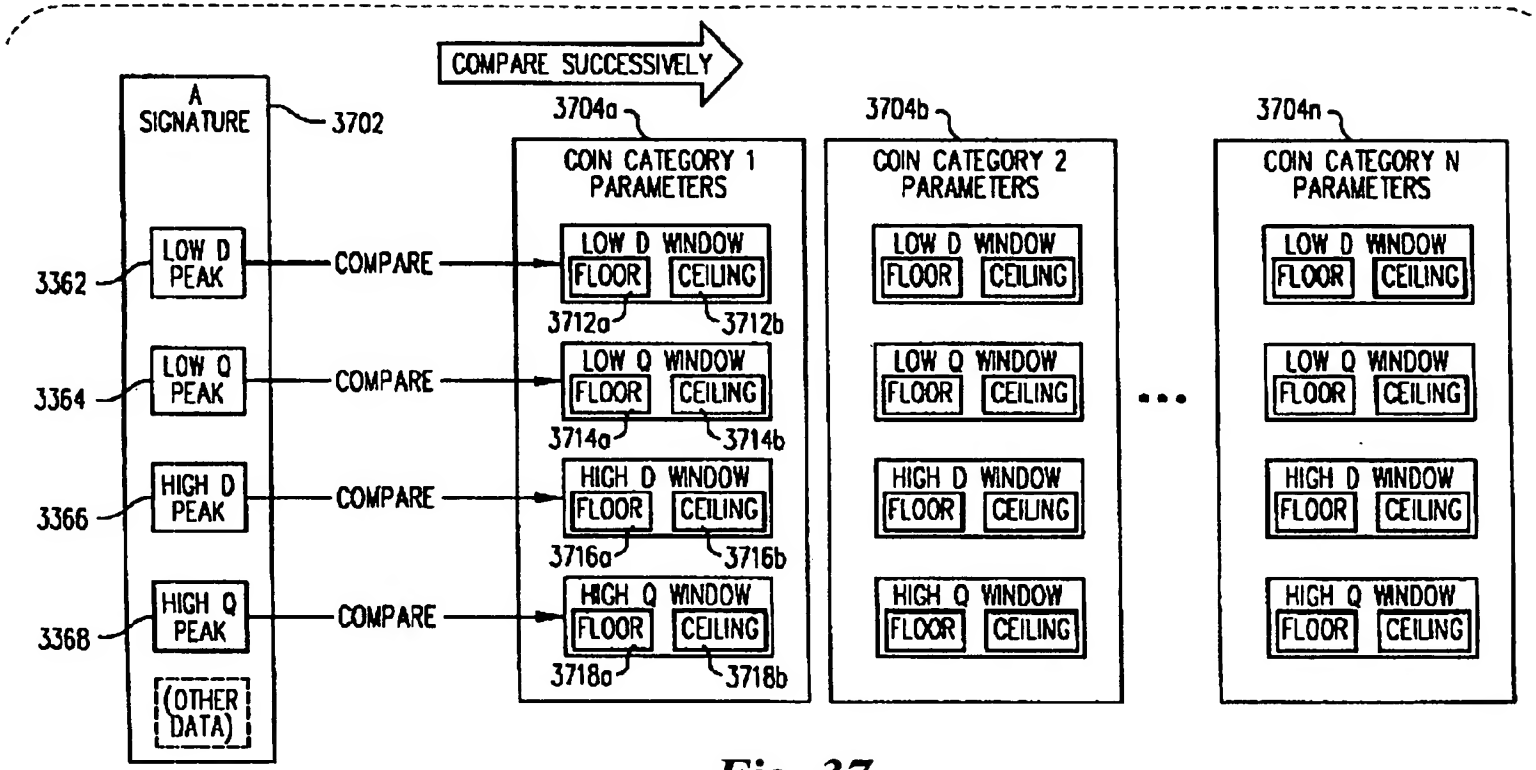

COMPARE SUCCESSIVELY
A SIGNATURE
3702
3704a
3704b
3704n
COIN CATEGORY 1 PARAMETERS
COIN CATEGORY 2 PARAMETERS
COIN CATEGORY N PARAMETERS
LOW D PEAK
LOW Q PEAK
HIGH D PEAK
HIGH Q PEAK
(OTHER DATA)
3362
3364
3366
3368
COMPARE
LOW D WINDOW
LOW Q WINDOW
HIGH D WINDOW
HIGH Q WINDOW
FLOOR
CEILING
3712a
3712b
3714a
3714b
3716a
3716b
3718a
3718b

Fig. 37

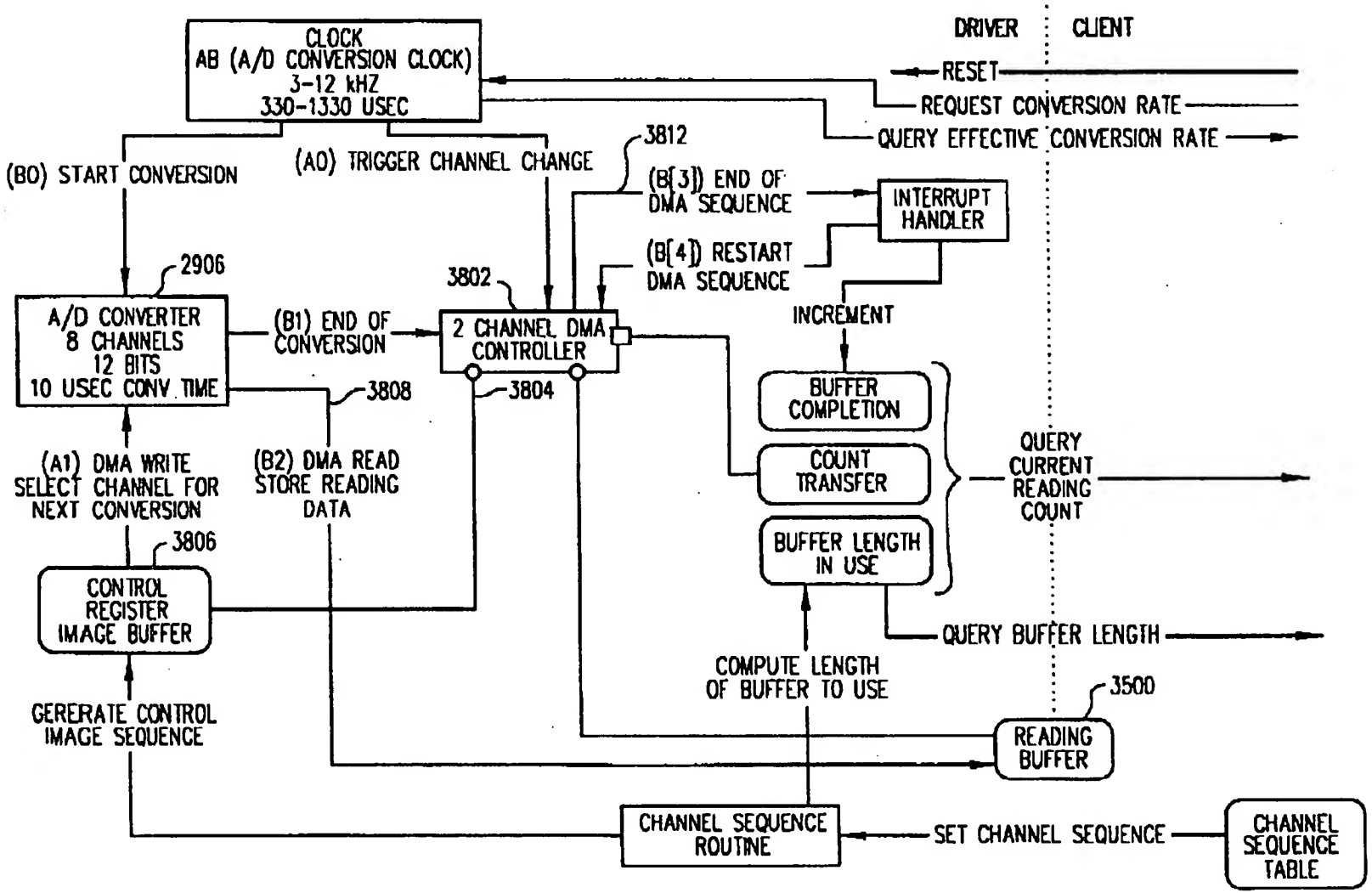

CLOCK
AB (A/D CONVERSION CLOCK)
3-12 kHZ
330-1330 USEC
DRIVER
CLIENT
RESET
REQUEST CONVERSION RATE
QUERY EFFECTIVE CONVERSION RATE
(BO) START CONVERSION
(AO) TRIGGER CHANNEL CHANGE
3812
(B[3]) END OF DMA SEQUENCE
INTERRUPT HANDLER
(B[4]) RESTART DMA SEQUENCE
2906
3802
A/D CONVERTER
8 CHANNELS
12 BITS
10 USEC CONV TIME
(B1) END OF CONVERSION
2 CHANNEL DMA CONTROLLER
INCREMENT
3808
3804
BUFFER COMPLETION
COUNT TRANSFER
BUFFER LENGTH IN USE
QUERY CURRENT READING COUNT
(A1) DMA WRITE SELECT CHANNEL FOR NEXT CONVERSION
(B2) DMA READ STORE READING DATA
3806
CONTROL REGISTER IMAGE BUFFER
QUERY BUFFER LENGTH
COMPUTE LENGTH OF BUFFER TO USE
3500
GERERATE CONTROL IMAGE SEQUENCE
READING BUFFER
CHANNEL SEQUENCE ROUTINE
SET CHANNEL SEQUENCE
CHANNEL SEQUENCE TABLE

Fig. 38

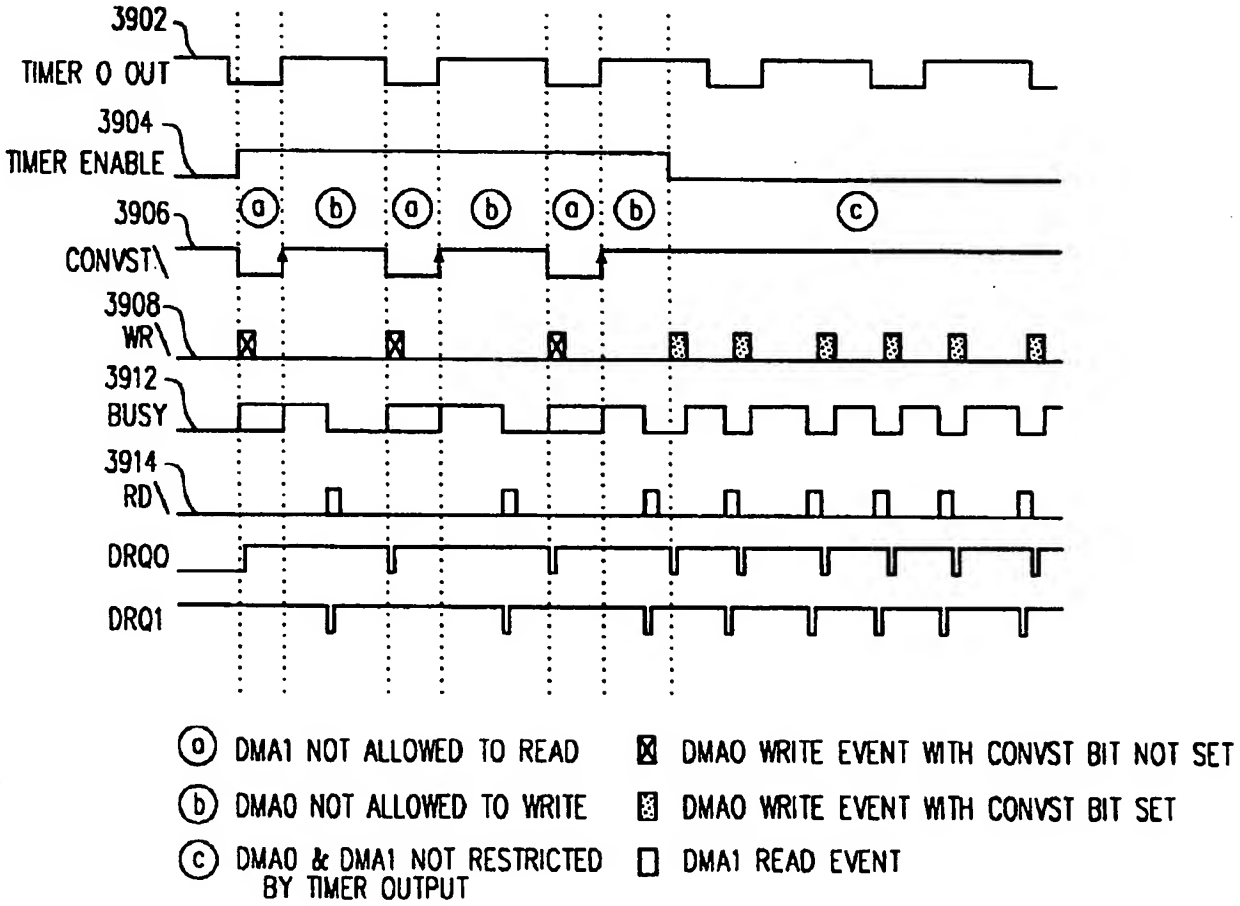

3902
TIMER 0 OUT
3904
TIMER ENABLE
3906
CONVST\
3908
WR\
3912
BUSY
3914
RD\
DRQ0
DRQ1
a
b
a
b
a
b
c
a DMA1 NOT ALLOWED TO READ
b DMA0 NOT ALLOWED TO WRITE
c DMA0 & DMA1 NOT RESTRICTED BY TIMER OUTPUT
DMA0 WRITE EVENT WITH CONVST BIT NOT SET
DMA0 WRITE EVENT WITH CONVST BIT SET
DMA1 READ EVENT

Fig. 39

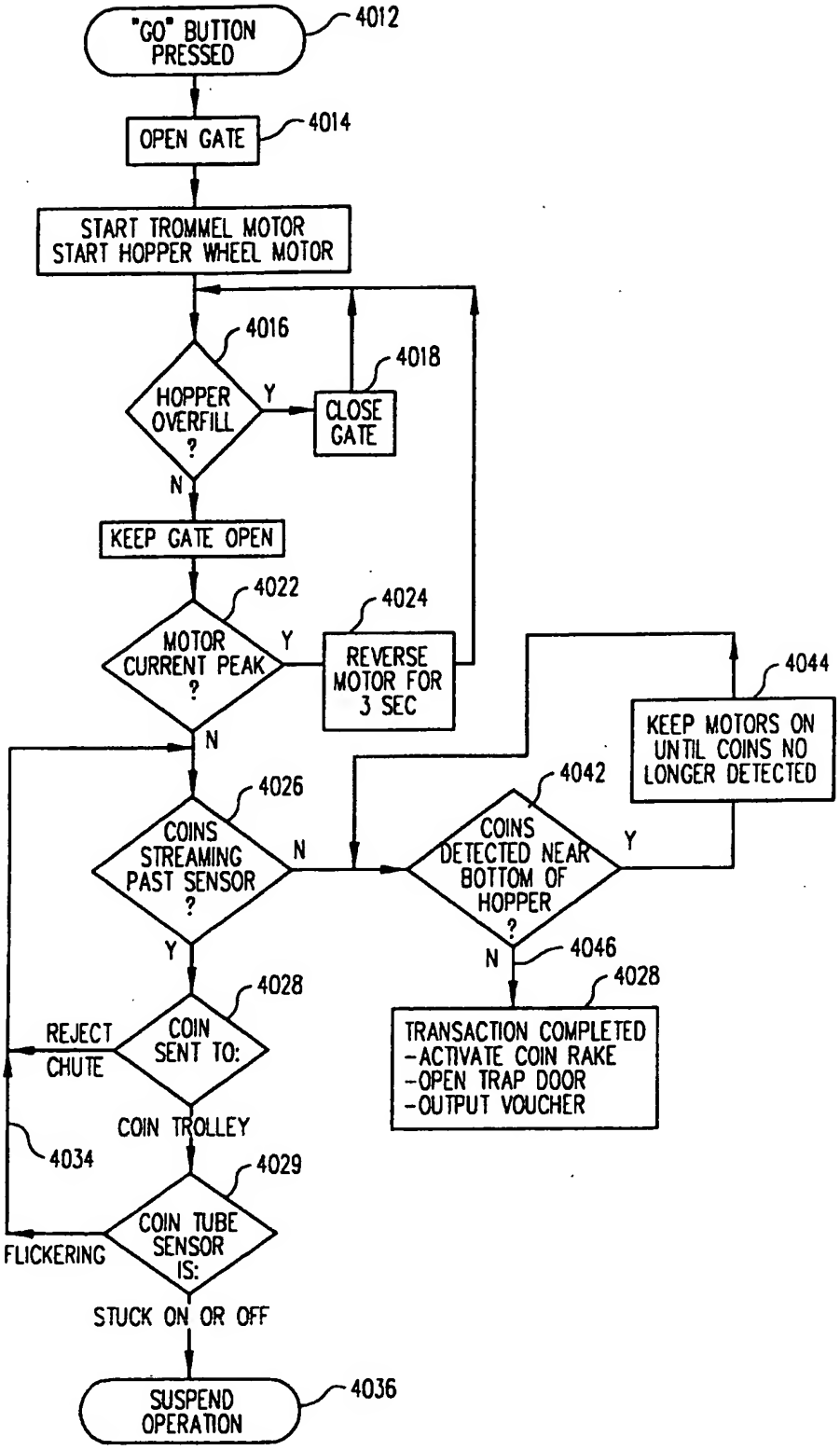

"GO" BUTTON PRESSED
4012
OPEN GATE
4014
START TROMMEL MOTOR
START HOPPER WHEEL MOTOR
4016
HOPPER OVERFILL ?
Y
4018
CLOSE GATE
N
KEEP GATE OPEN
4022
MOTOR CURRENT PEAK ?
Y
4024
REVERSE MOTOR FOR 3 SEC
N
4026
COINS STREAMING PAST SENSOR ?
N
4042
COINS DETECTED NEAR BOTTOM OF HOPPER ?
Y
4044
KEEP MOTORS ON UNTIL COINS NO LONGER DETECTED
Y
N
4046
4028
TRANSACTION COMPLETED
-ACTIVATE COIN RAKE
-OPEN TRAP DOOR
-OUTPUT VOUCHER
4028
REJECT CHUTE
COIN SENT TO:
COIN TROLLEY
4034
4029
COIN TUBE SENSOR IS:
FLICKERING
STUCK ON OR OFF
SUSPEND OPERATION
4036

Fig. 40

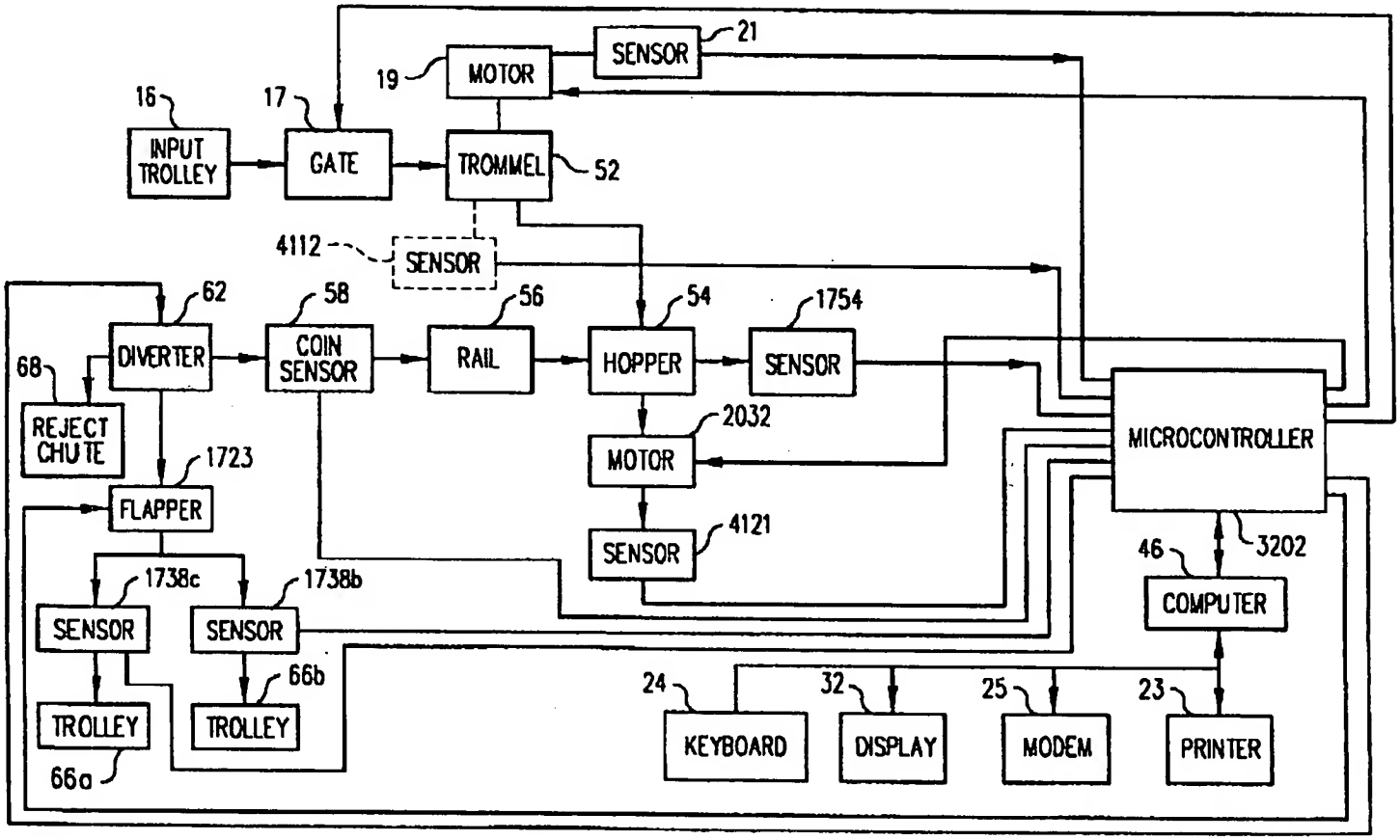

16
INPUT TROLLEY
17
GATE
19
MOTOR
SENSOR
21
TROMMEL
52
4112
SENSOR
62
DIVERTER
58
COIN SENSOR
56
RAIL
54
HOPPER
1754
SENSOR
68
REJECT CHUTE
1723
FLAPPER
2032
MOTOR
4121
SENSOR
MICROCONTROLLER
46
COMPUTER
3202
1738c
SENSOR
1738b
SENSOR
66b
TROLLEY
66a
TROLLEY
24
KEYBOARD
32
DISPLAY
25
MODEM
23
PRINTER

Fig. 41

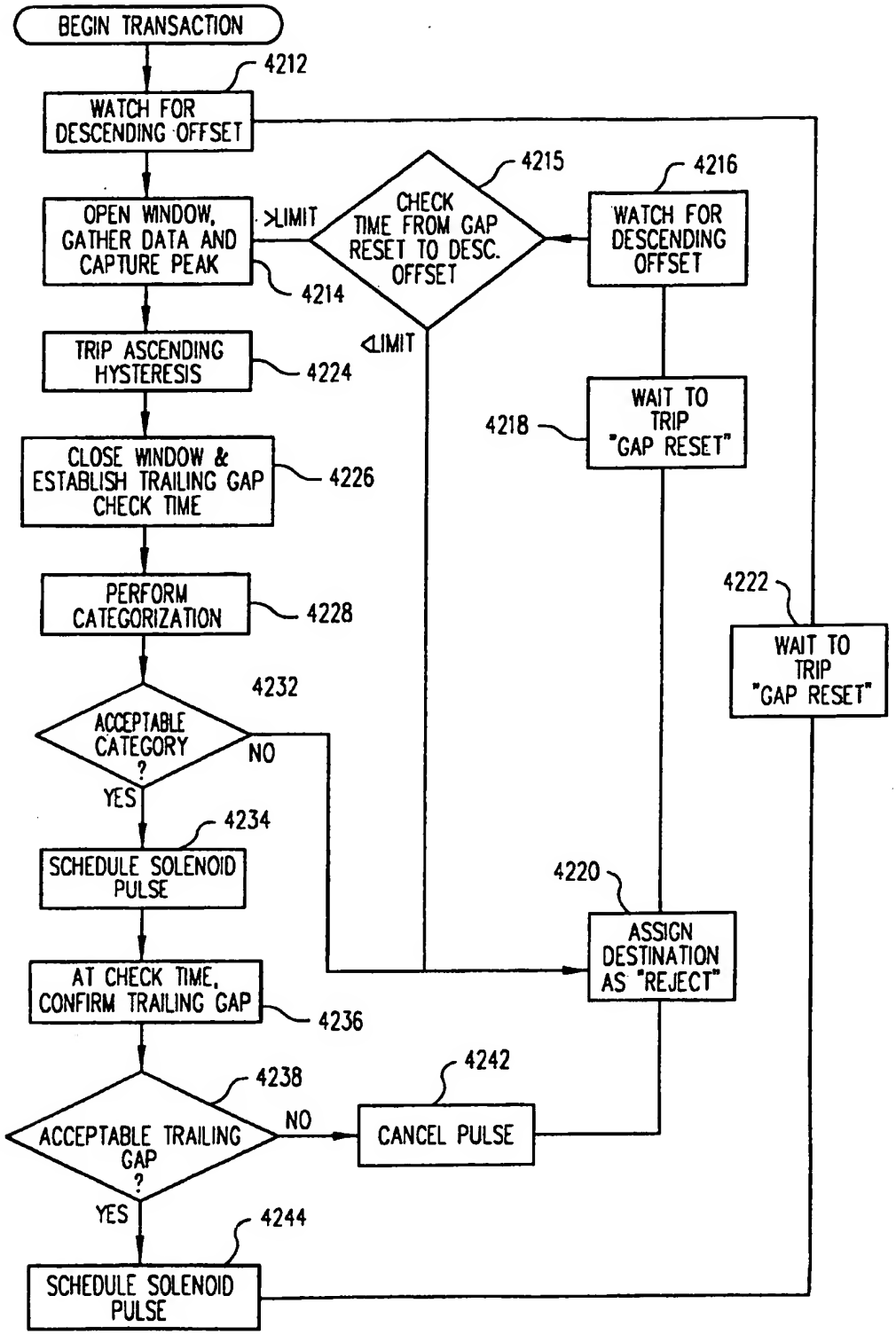

BEGIN TRANSACTION
4212
WATCH FOR DESCENDING OFFSET
OPEN WINDOW, GATHER DATA AND CAPTURE PEAK
>LIMIT
4214
CHECK TIME FROM GAP RESET TO DESC. OFFSET
4215
4216
WATCH FOR DESCENDING OFFSET
<LIMIT
TRIP ASCENDING HYSTERESIS
4224
WAIT TO TRIP "GAP RESET"
4218
CLOSE WINDOW & ESTABLISH TRAILING GAP CHECK TIME
4226
PERFORM CATEGORIZATION
4228
4222
WAIT TO TRIP "GAP RESET"
ACCEPTABLE CATEGORY ?
4232
NO
YES
SCHEDULE SOLENOID PULSE
4234
4220
ASSIGN DESTINATION AS "REJECT"
AT CHECK TIME, CONFIRM TRAILING GAP
4236
ACCEPTABLE TRAILING GAP ?
4238
NO
4242
CANCEL PULSE
YES
SCHEDULE SOLENOID PULSE
4244

Fig. 42

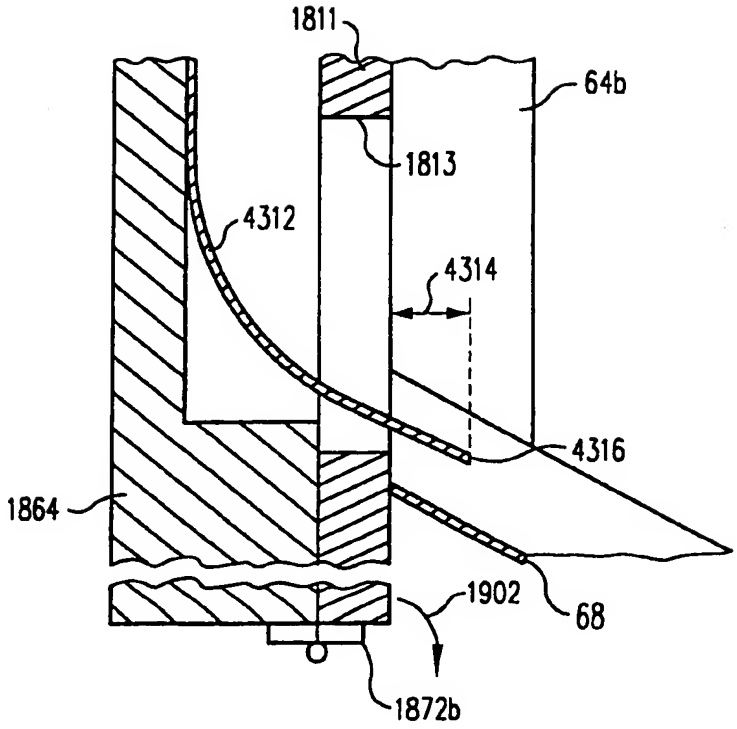


Fig. 43

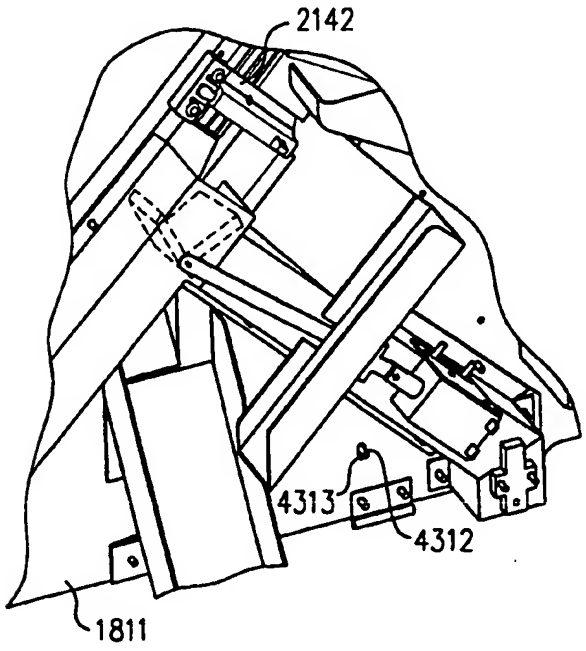


Fig. 43A

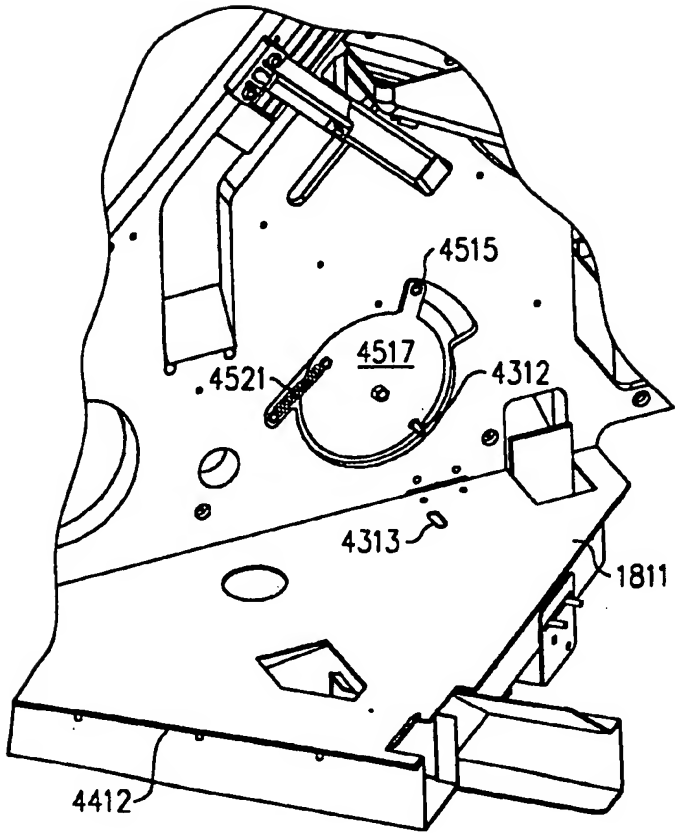


Fig. 44

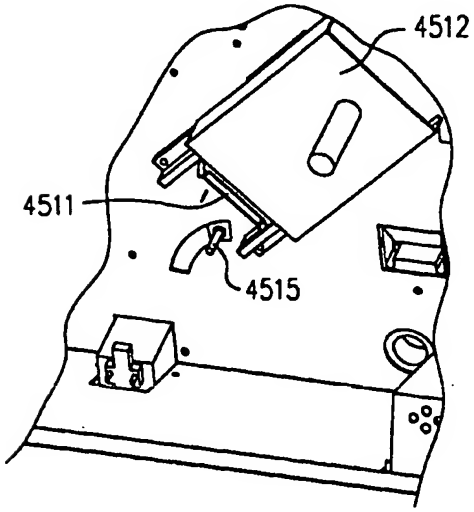


Fig. 45

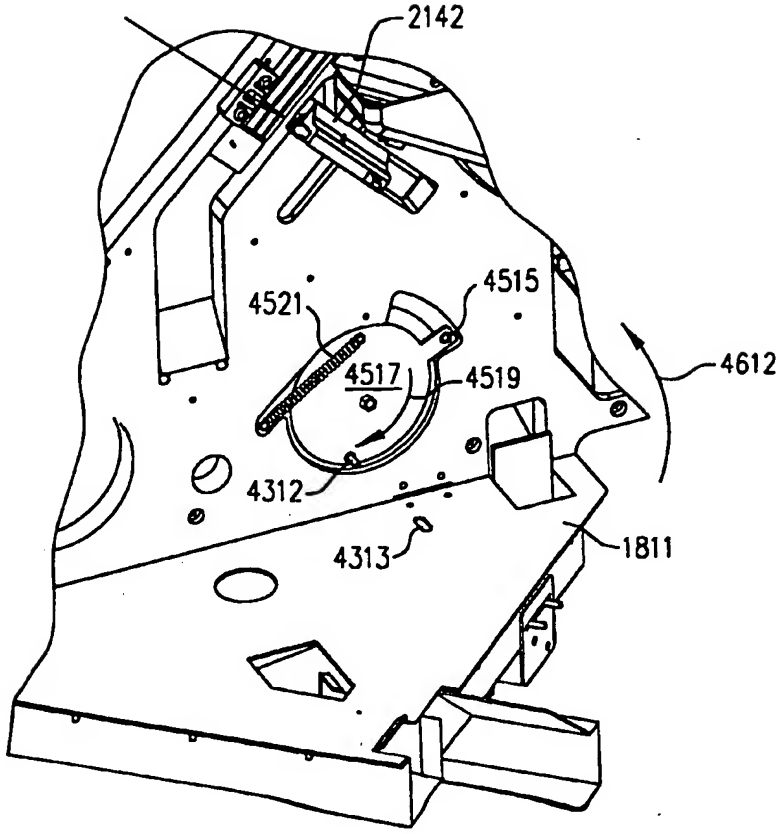


Fig. 46

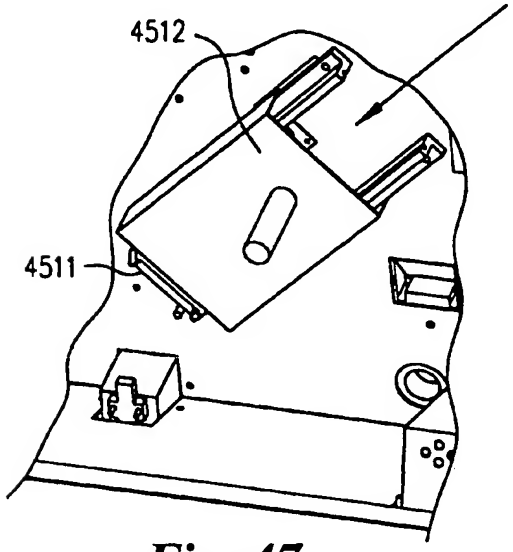


Fig. 47

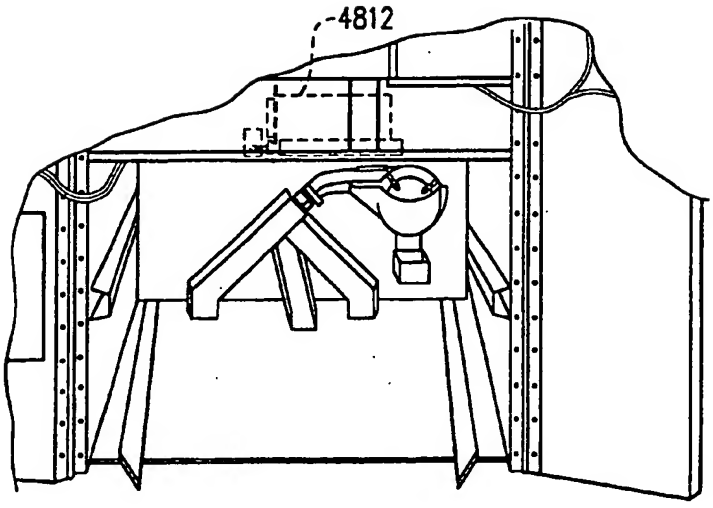


Fig. 48

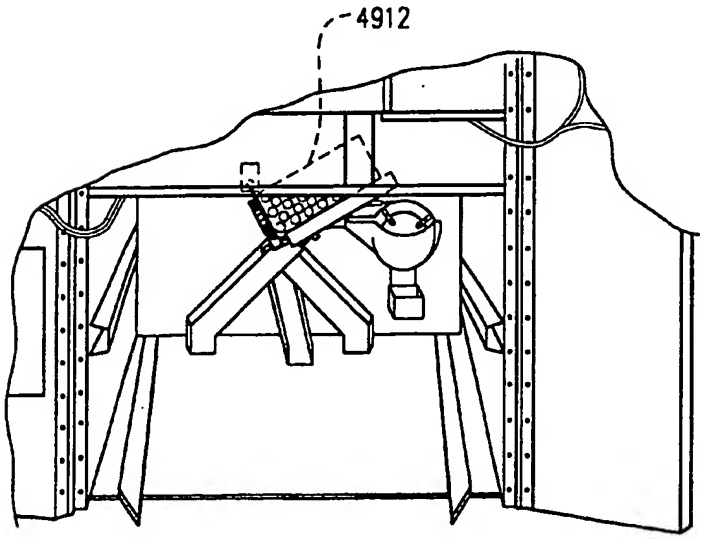


Fig. 49

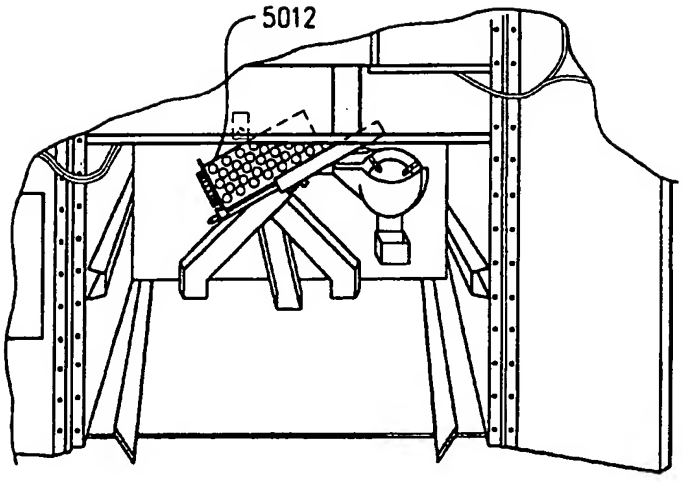


Fig. 50

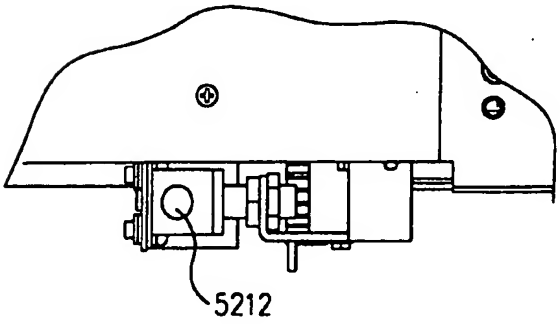


Fig. 52

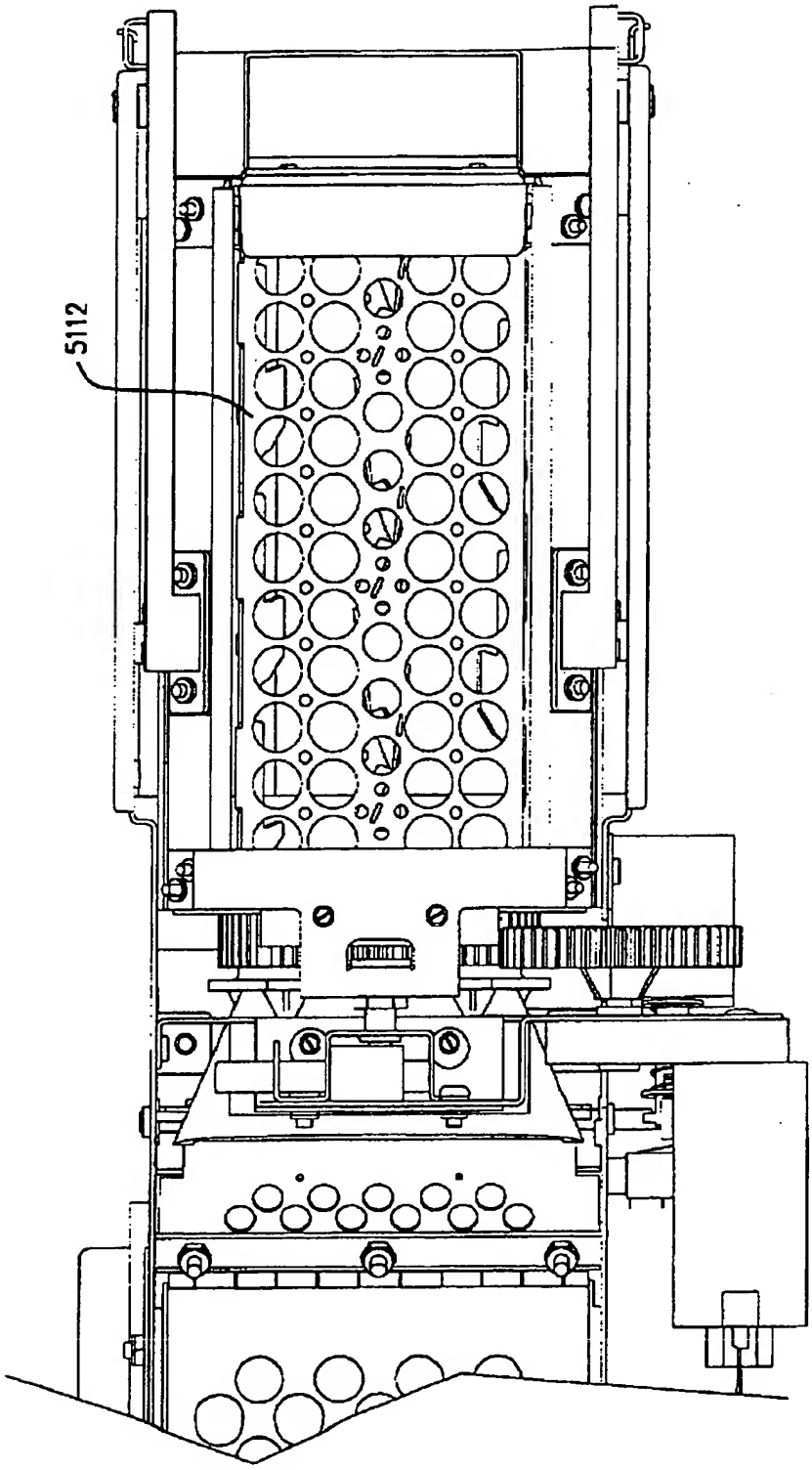


Fig. 51

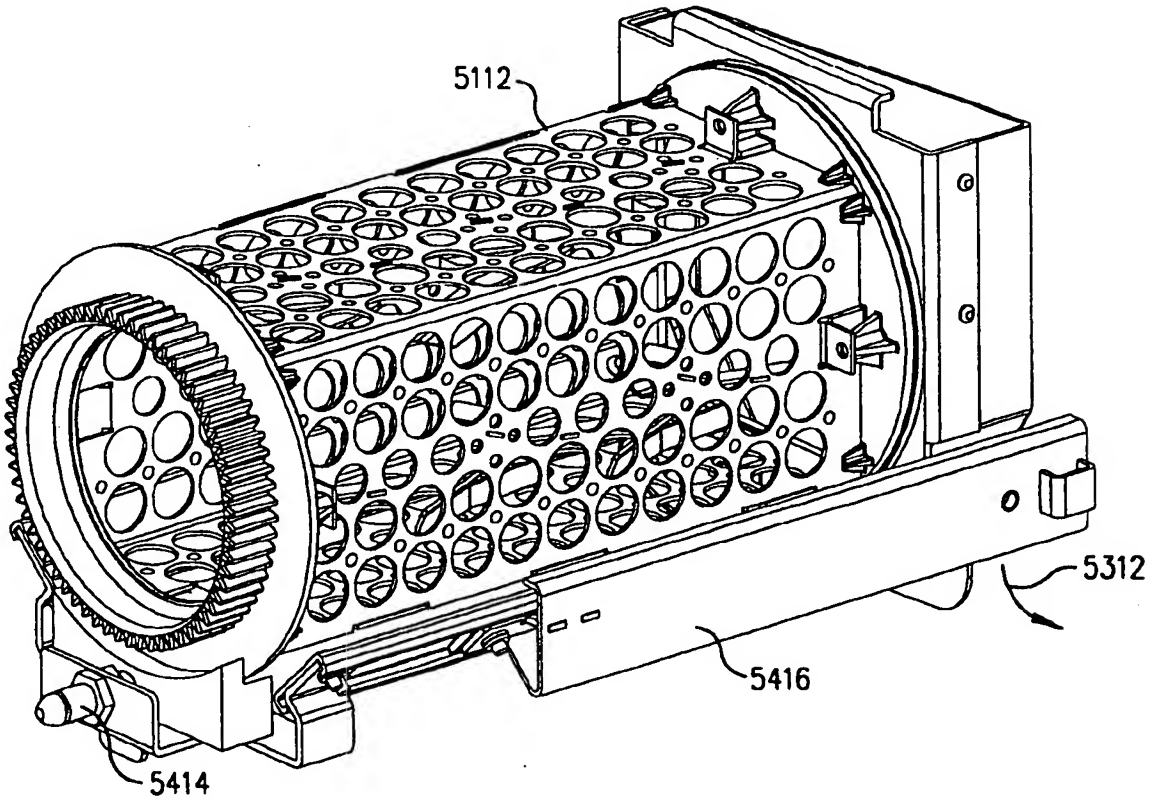


Fig. 53

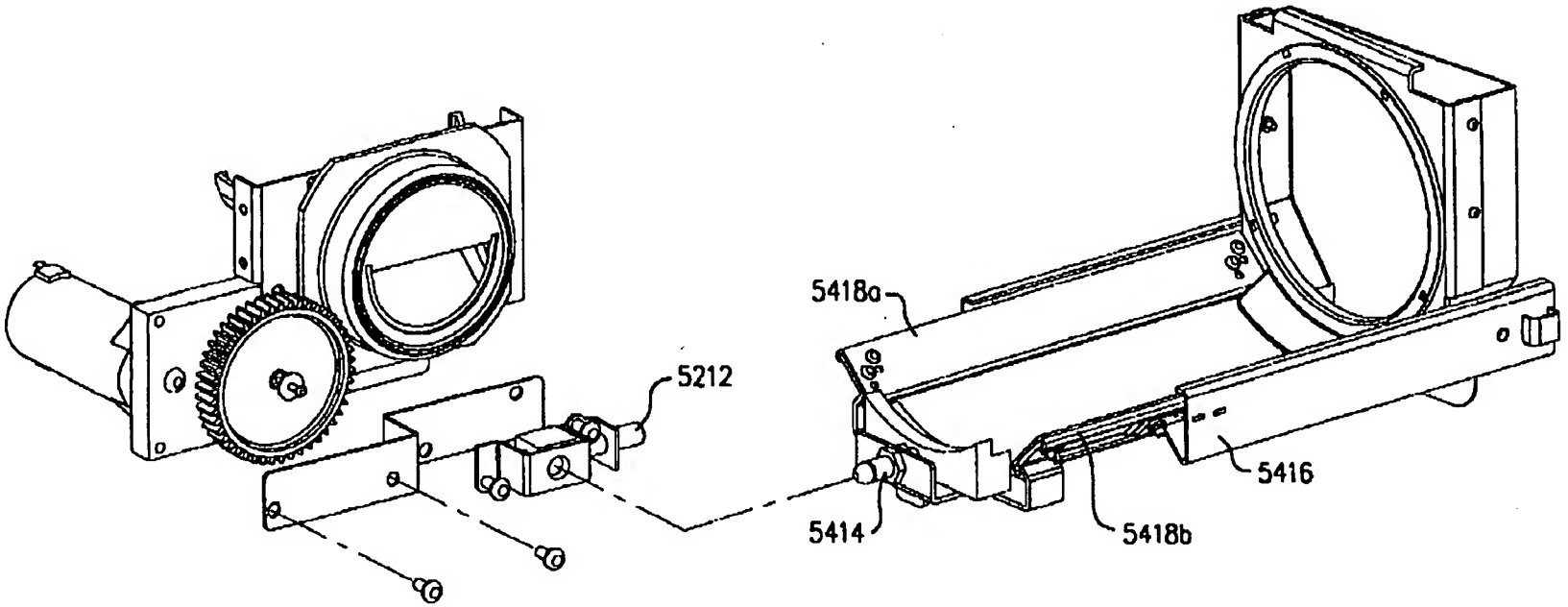


Fig. 54

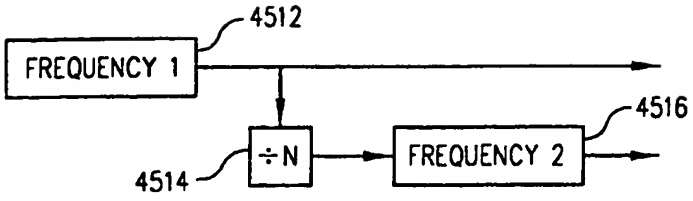


Fig. 55A

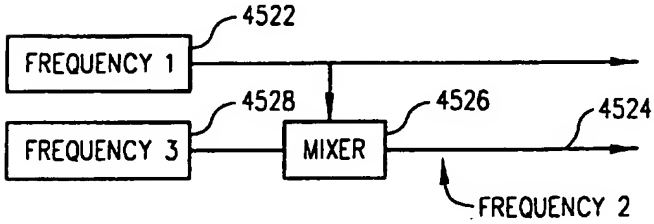


Fig. 55B

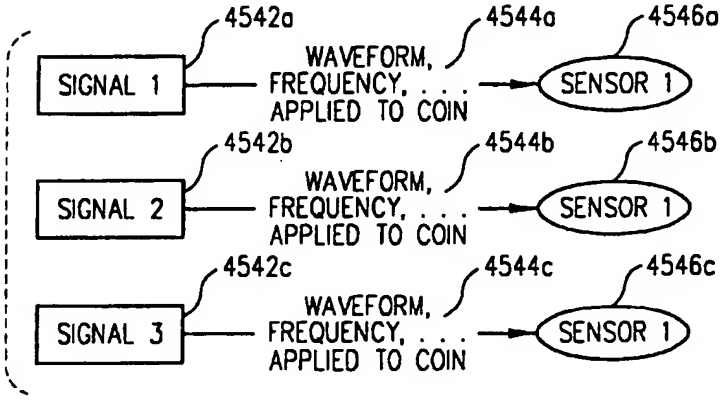


Fig. 55C

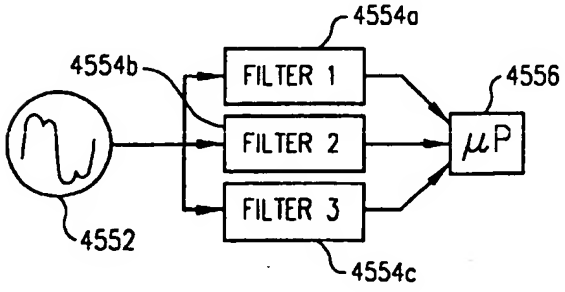


Fig. 55D

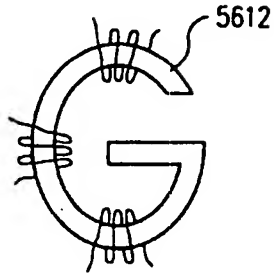


Fig. 56A

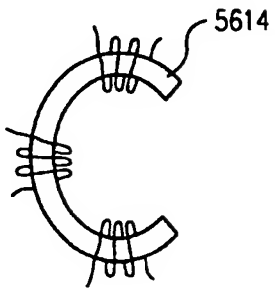


Fig. 56B

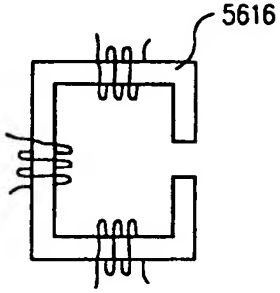


Fig. 56C

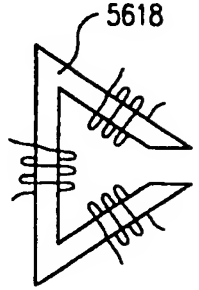


Fig. 56D

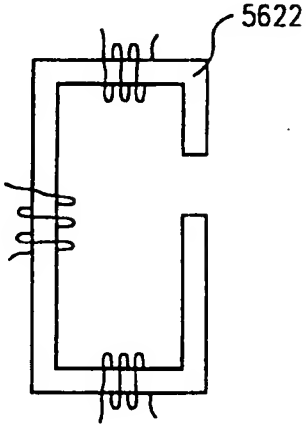


Fig. 56E

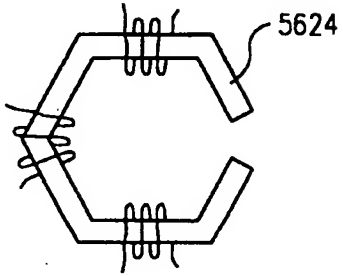


Fig. 56F

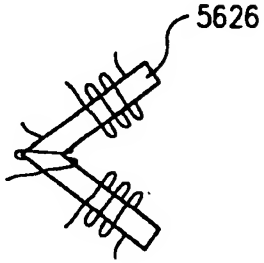


Fig. 56G

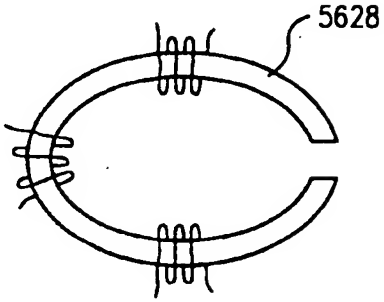


Fig. 56H